Silicon Valley Polytechnic Institute®, Inc.

SCHOOL CATALOG

FOR

CALENDAR YEAR

2023

January 1, 2023- to December 31, 2023

1754 Technology Drive, Suite 228
San Jose, CA 95110

Silicon Valley Polytechnic Institute, Inc.

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www.SVPTI.com

This catalog is valid from January 1, 2023- to December 31, 2023. It is updated annually.

THE MISSION, PURPOSES

It is the mission of the Silicon Valley Polytechnic Institute, Inc. (SVPTI) to achieve and maintain a position as a leading training provider serving the electronic and computer industries. SVPTI strives to provide students with a fostering, productive and professional training environment that maximizes the learning process. The instruction provided for students is high quality and highly individualized. It is intended to develop and enhance the knowledge and demanding skills required in these exceptionally dynamic fields.

SVPTI intends to achieve its mission by offering highly useful non-degree certificate and diploma programs using relevant, focused and advanced curricula, a high level of student – instructor interaction, small class sizes and highly qualified faculty with years of direct industry experience.

Silicon Valley Polytechnic Institute, Inc. strives to provide students with a fostering, productive and professional training environment that maximizes the learning process. The instruction provided for students is high quality and highly individualized. It is intended to develop and enhance the knowledge and demanding skills required in these exceptionally dynamic fields.

Non-Degree programs at present include over 60 programs. Representative programs include: Computer Aided Design and Drafting with AutoCAD; Advanced and 3D Computer Drafting and Design with AutoCAD; Computer Aided Design and Drafting with SolidWorks: Advanced Computer Aided Design and Drafting with SolidWorks; Digital VLSI Design with Verilog; Timing Verification of Digital VLSI Designs; Design of Analog CMOS Integrated Circuits; and Design of Radio Frequency Integrated Circuits. A complete list of all programs approved by BPPE to date are included in this catalog.

Students at SVPTI are predominantly working professionals who already often have diplomas and degrees. These students have typically been employed for a period of at least 2 to as much as 20 years.

SVPTI primarily serves the demographic above because there are dynamic changes in the industrial sector to the extent that employees need to periodically update and re-tool their knowledge and skills.

SVPTI intends to maintain strong ties with the electronic, computer and Internet industries to constantly improve its training products and procedures and to be responsive to the needs of these changing industries. It is anticipated that an Industry Advisory Committee will be established perhaps within the first year of operations.

SVPTI is careful not to make specific occupation or job guarantees or promises of placement made upon graduation from a course or program. Obviously, there are a range of occupations or titles to which such training may lead. Though no specific guarantees of employment and no promises of placement are made, there are numerous related occupations or job titles that require such knowledge and skills provided through the courses and programs at SVPTI.

Students do not need to be licensed technicians or engineers to obtain a large number of available jobs in the general field of engineering and manufacturing. Representative

occupations for which graduates of SVPTI programs would be qualified include the following fields:

- Analog Design Engineering
- Radio Frequency and Integrated Circuits Engineering (RFIC)
- Digital Design Engineering
- Computer Aided Design Drafting
- Computer Aided Design Drafting – Mechanical Engineering
- Computer Aided Design Drafting – Architectural Engineering

It is the policy of SVPTI that all newly enrolled students will have easy access to this catalog as part of their enrollment process. The catalog will be available online for ready reference, or, if the student wishes to obtain a hard copy of the catalog, one will be provided upon request. SVPTI recognizes that an enrollment agreement is not valid unless student has access to current school catalog prior to signing for the training.

Additionally, the policy of SVPTI is that the school catalog will be annually updated as necessary with catalog addenda. However, all catalogs will otherwise be updated and republished as a new edition every year. The period covered by any particular catalog will be clearly stated on the cover/title page of the catalog.
In addition to receiving the school catalog, which contains outline of all training programs, if necessary students might receive a program specific brochure from school and/or from the program's instructor if available.

As a prospective student, you are encouraged to review this catalog prior to signing an enrollment agreement. You are also encouraged to review the School Performance Fact Sheet which must be provided to you prior to signing an enrollment agreement.

Silicon Valley Polytechnic Institute, Inc. is a private institution, and it is approved to operate by the Bureau for Private Postsecondary Education (BPPE), and that approval means compliance with state standards as set forth in the CEC and 5, CCR. Any questions a student may have regarding this catalog that has not been answered by the institution may be directed to the Bureau for Private Postsecondary Education at:

Bureau for Private Postsecondary Education
1747 North Market Blvd., Suite 225, Sacramento, CA 95834
www.bppe.ca.gov
Phone: (916) 574-8900
Toll Free: (888) 370-7589
Fax (916) 263-1897A

student or any member of the public may file a complaint about this institution with the Bureau for Private Postsecondary Education by calling the toll-free telephone #: (888) 370-7589 or by completing a complaint form, which can be obtained on the bureau's internet Web site www. bppe.gov

Additionally the Office of Student Assistance and Relief (OSAR) is available to support prospective students, current students, or past students of private postsecondary educational institutions in making informed decisions, understanding their rights, and

navigating available services and relief options. The office may be reached by calling the Toll-free telephone # (888) 370-7589, Website address: www.osar.bppe.ca.gov.

PROGRAMS OF INSTRUCTION

Silicon Valley Polytechnic Institute, Inc. offers over sixty courses of instruction. Many of the program offerings are centered on the subject area of electrical engineering and software development but we do offer several Computer Aided Drafting (CAD) courses, and manufacturing related programs as well. Please see Appendix-II for a complete list of all training programs, including duration, clock hours, and tuition.
Most of the programs are 12 weeks (120 Hours) in length but there are also 6 weeks and 8 weeks programs available. Please see appendix-II for more detail.
There are no requirements for licensure to work in any of the subject areas of instruction.

All trainings are conducted at Silicon Valley Polytechnic, Inc. Facility located at 1754 Technology Drive, Suite 228, San Jose, CA 95110.

Up to date list of current programs of instruction approved by BPPE is posted in BPPE website at https://app.dca.ca.gov/bppe/view-school.asp?schlcode=67964704 and is shown below:

3D MICROELECTRONIC SYSTEM INTEGRATION
ADVANCED 3D COMPUTER AIDED DESIGN AND DRAFTING WITH SOLIDWORKS
ADVANCED ANALOG CMOS IC DESIGN
ADVANCED AND 3D COMPUTER DRAFTING AND DESIGN WITH AUTOCAD
ADVANCED PCB LAYOUT DESIGN
ADVANCED RFIC DESIGN
ADVANCED SEMICONDUCTOR DEVICES - PHYSICS & TCAD
ADVANCED SEMICONDUCTOR TECHNOLOGY AND FABRICATION
ADVANCED SOLAR PHOTOVOLTAIC SYSTEM DESIGN
APPLIED ELECTRICITY AND ELECTRONICS FUNDAMENTALS
AUTODESK REVIT ARCHITECTURE ESSENTIALS
AUTOMATED SOFTWARE TESTING WITH SELENIUM IDE
AUTOMATED TEST AND MEASUREMENT WITH LABVIEW
C PROGRAMMING ESSENTIALS
C++ PROGRAMMING ESSENTIALS
CATIA DRAFTING ESSENTIALS
COMPUTER AIDED DESIGN AND DRAFTING WITH AUTOCAD
COMPUTER AIDED DESIGN AND DRAFTING WITH SOLIDWORKS
COMPUTER AND NETWORK SECURITY ESSENTIALS
COMPUTER NETWORKING FUNDAMENTALS
CUSTOM PHYSICAL DESIGN ESSENTIALS
CYBERSECURITY FOUNDATIONS
CYBERSECURITY IMPLEMENTATION
DESIGN OF ANALOG CMOS INTEGRATED CIRCUITS
DESIGN OF DIGITAL CMOS INTEGRATED CIRCUITS
DESIGN OF LOW POWER DIGITAL INTEGRATED CIRCUITS
DESIGN OF RADIO FREQUENCY INTEGRATED (RFIC) CIRCUITS
DESIGN SIGNAL PROCESSING PRINCIPLES AND APPLICATIONS
DIGITAL LOGIC DESIGN FUNDAMENTALS

DIGITAL MANUFACTURING & INDUSTRY 4.0 ESSENTIALS
DIGITAL SIGNAL PROCESSING WITH MATLAB
DIGITAL VLSI IC DESIGN WITH VERILOG
EMBEDDED SYSTEM DESIGN FUNDAMENTALS
FPGA DESIGN FUNDAMENTALS
FULL STACK SOFTWARE DEVELOPMENT ESSENTIALS
HTML & CSS ESSENTIALS
IC LAYOUT DESIGN
IC LAYOUT VERIFICATION
IC PACKAGING DESIGN ESSENTIALS
IC PACKAGING FUNDAMENTALS
INTERNET OF THINGS (IOT) DESIGN & APPLICATION
INTERNET OF THINGS (IOT) FUNDAMENTALS
JAVA PROGRAMMING ESSENTIALS
JAVASCRIPT ESSENTIALS
LOW POWER VLSI DESIGN
MATLAB FOR ENGINEERING AND SCIENTIFIC APPLICATIONS
MECHANICAL DRAFTING FUNDAMENTALS
MEM DESIGN & TECHNOLOGY FUNDAMENTALS
NATIONAL ELECTRICAL CODE (NEC) TRAINING
PCB AND PWB TECHNOLOGY FUNDAMENTALS
PCB LAYOUT DESIGN
PHP/MYSQL PROGRAMMING ESSENTIALS
PHYTON PROGRAMMING ESSENTIALS
PRACTICAL DESIGN WITH DSP
PRODUCT MANAGEMENT ESSENTIALS
PROFESSIONAL SCRUM DEVELOPER
PROFESSIONAL SCRUM MASTER LEVEL II
PROJECT MANAGEMENT ESSENTIALS
REVIT ARCHITECTURE COMMERCIAL AND MEP
SCRUM MASTER AND JIRA TRAINING
SCRUM MASTER BOOTCAMP
SKETCHUP ESSENTIALS
SOFTWARE QUALITY ASSURANCE ESSENTIALS
SOLAR PHOTOVOLTAIC DEVICE PHYSICS
SOLAR PHOTOVOLTAIC SYSTEM DESIGN ESSENTIALS
TIMING VERIFICATION OF DIGITAL VLSI DESIGNS
VLSI PHYSICAL DESIGN ESSENTIALS

Though various components of instruction can be supplemented by referencing the same subject matter on the Internet, all instruction at SVPTI is very much a combination of lecture and “hands on” instruction considered as “in residence” or face-to-face instruction.

These programs of instruction are described in much more detail on the following pages.

Pre-Enrollment Disclosure; Notice to Prospective Degree Program Students
Silicon Valley Polytechnic Institute, Inc. does not offer any degreed programs.

California Education Code Section 94909(a)(16)

Silicon Valley Polytechnic Institute, Inc. does not offer any degree program and is not accredited by an any accrediting agency recognized by the United States Department of Education.

SVPTI Programs
Appendix I of this catalog includes detail description of all the courses offered, as well as description of the instruction for each course offered by SVPTI. Appendix II shows the total duration, clock hours tuition and fees for each course. A training programs can consist of one or several of the courses taken together. All information regarding these courses is provided in Appendix-II.

SCHEDULE OF TOTAL CHARGES

Pursuant to CEC 94909(a)(9) the schedule of total charges for a period of attendance AND an estimated schedule of total charges for the entire educational program is shown for each one of the courses offered by the institute in Appendix-II of this catalog. All the charges are due and payable prior to the start of training.

FACULTY AND QUALIFICATIONS

Among other things, California Code of Regulations Section 71720 states that an institution must employ duly qualified faculty in sufficient numbers to provide the instruction, student advisement, and learning outcomes evaluation necessary for the institution to document its achievement of its stated mission and objectives, and for students to achieve the specific learning objectives of each course offered.

It requires each institution to develop and implement written policies and procedures providing for the participation of duly qualified faculty in the conducting of research, development of curricula, academic planning, enforcement of standards of academic quality, pursuit of academic matters related to the institution's mission and objectives, establishment of criteria for contracting with new faculty, and evaluation of faculty credentials.

This section provides that the institution shall base its faculty requirements on all of the following factors:

1. The educational level and number of students;
2. The number of hours needed for direct interaction between students and faculty per course, quarter, semester, or other term;
3. The number of hours needed to be spent on evaluating written materials prepared by students, such as lessons, papers, and examinations, per course, quarter, semester, or other term;
4. The number of group meetings per course, quarter, semester, or other term;
5. The faculty duties established by the institution as required; and
6. The number of hours per week or units per term considered full-time for faculty in the institution. This section further provides that faculty shall possess sufficient expertise to support the institution's award of its degrees or diplomas, and that the faculty as a whole shall possess a

diverse educational background. This diverse background shall be demonstrated by earned degrees from a variety of colleges and universities or by credentials generally recognized in the field of instruction.

Records document that each faculty member is duly qualified and was qualified to perform the duties to which they were assigned including providing instruction, and evaluating learning outcomes.

Appendix –IV of this catalog includes a listing and qualification of additional faculty members.

Instruction will take place on the school premises located at 1754 Technology Drive, Suite 228, San Jose, CA. Instructors will of course be present at the school location when teaching, but instructors will also be available to meet with students outside of or in addition to class time during mutually agreed upon meeting times each week.

Due to the nature of the material covered, and the relatively small number of students per course, on average and across courses, this is expected to involve perhaps one additional hour per course per week.

ADMISSION REQUIREMENTS

For approved Non-Degree programs, SVPTI will require applicants to have a high school diploma or its equivalent GED (General Education Diploma).

All applicants will be required to be at least 17 years of age by the commencement date of the first class in which they enroll. Documentation of age may be required.
SVPTI does not offer ability-to-benefit to students and does not conduct ability-to-benefit examinations.

Prospective students will meet with a SVPTI admissions representative on campus. All applicants must complete an application form. The representative will provide information about programs, schedules, tuition and fees.

Since all instructions at SVPTI are in English, all applicants must demonstrate the ability to communicate in English, at least at high US high school level. This is achieved through the interview process, conducted by school official during the school visit by the prospective student. If there is sufficient doubt about the applicant's ability to communicate in English, a TOEFL (Test of English as a Foreign Language) test score result of at least 500 or higher will need to be documented by the applicant.

If an applicant's test score is below the 500 level on the TOEFL exam, or if they simply so choose, they will have the option to enroll in an ESL program at another institution at the appropriate level of instruction. Successful completion of the ESL Intermediate level program for such students will be required before they may enroll in any course at SVPTI.

It is anticipated that a basic knowledge of mathematics could be demonstrated through the Wonderlic Basic Skills Test, or preferably, through documentation of graduation from high school or possession of a GED Certificate.

Applicants will need basic familiarity with using computers as a prerequisite to register for any course.

SVPTI is committed to a policy of non-discrimination in admissions and will not refuse service to any qualified individual based on color, sex, religion, or national origin.

Applicants will be advised that the use of color coding is one prominent method used as a standard in the industry for coding electronic components and drawings. Therefore, color-blind individuals may have difficulty in some courses.

Since SVPTI does not provide any financial assistance, it will be incumbent upon applicants to demonstrate the availability of sufficient financial sources to pay for their course of instruction. A registration fee of $150 must accompany the Application for Admission. The balance of tuition must be paid prior to the first session of instruction.

The signed enrollment agreement will not become effective until the prospective student attends the first class or session of instruction.

SVPTI does not offer or provide any degree programs. All program offerings are Non-Degree or vocational in nature. Consequently, no postsecondary general education courses are required, nor will any be offered.

For all Non-Degree coursework, the Silicon Valley Polytechnic Institute, Inc. will assess and evaluate student performance in order to grant a passing or failing grade. The Silicon Valley Polytechnic Institute, Inc. will require that a student earn at least a C average (2 points on a 4 points scale) in order to satisfactorily complete a course of instruction.

As can be referenced in the course syllabi, a student must attain an earned average of no less than 60% to pass a course of instruction. For all Non-Degree coursework, SVPTI will assess and evaluate student performance in order to grant a grade of A, B, or C. SVPTI will require that a student earn at least a D average (1 point on a 4 points scale) in order to satisfactorily complete a course of instruction.

The basic grading standard will be:

A	90% - 100%
B	80% - 89%
C	70% - 79%
D	60% - 69%
F	Below 60%

Grades will be based on predominantly objective criteria such as exam results, projects, presentations, maintaining attendance, participation in class and engagement with the material.

SVPTI does not accept credits from other institutions, and has no articulation agreement with any other schools allowing the automatic acceptance of credit earned at any other institution. As a result, SVPTI has no specific policies or procedures for the award of credit for prior experiential learning.

Scholastic Regulations:

In order to maintain satisfactory progress as established by SVPTI, a student must maintain attendance (as explained below), perform satisfactorily throughout the program, and meet the minimum criteria established for completing the program.

Attendance Policies:

Students must maintain successful attendance. Each student is expected to attend every meeting of every class in which they are enrolled. Attendance will be recorded during each class.

Absenteeism may result in a warning, suspension, or dismissal. SVPTI will require a minimum attendance of at least 80% of all classes in order to complete a course. Individual instructors, however, can require a higher standard in their classes. Individual instructors will determine warning, suspension, and dismissal thresholds within this basic guideline.

Any work missed must be made up within the basic policy for attendance set forth by the instructor. Individual instructor policies must operate within the SVPTI standard for attendance. Students are responsible for all make-up work as a result of any missed classes. It is the student's responsibility to contact the appropriate faculty member(s) concerning possible make-up work. Make-up work will be at the discretion of each instructor.

Students are expected to be present at the beginning of each class session. It will be the student's responsibility to inform that instructor after class if they arrive after attendance is recorded.

Absence of 3 consecutive sessions without notification will result in an assumption of student withdrawal.

Dismissal and Suspension Policies:

SVPTI reserves the right to suspend or terminate any student whose conduct is deemed inappropriate and disruptive to instruction. Such conduct includes: excessive absences or tardiness; failure to maintain satisfactory progress; inappropriate behavior toward another student or staff member; failure to abide by school rules and regulations; failure to meet financial obligations; any other conduct deemed sufficiently disruptive of instruction so that, in the estimation of the instructor and CEO/President, continued instruction is not a reasonable or constructive proposition.

Students who have been suspended or terminated may request reinstatement in writing to the CEO/President after a period of at least thirty days.

A student may request and be granted a Leave of Absence in exceptional circumstances wherein it is determined to be impossible or unlikely that the student will be able to maintain attendance or satisfactory progress for a given period of time. A Leave of

Absence may be granted for sufficient cause by written petition to the instructor and/or CEO/President. The CEO/President will discuss the situation with the instructor, and, with benefit of the instructor's recommendation, authorize a Leave of Absence of no more than three months.

Any situation requiring a student absence or suspension longer than three months will necessitate the withdrawal of the student and any appropriate refunds.

TARDINESS

The Silicon Valley Polytechnic Institute, Inc. is a serious training program designed to maximize every moment of instruction and interaction between student and instructor. The instructor takes the program of instruction very seriously, and it is expected that the student will do so as well. At the same time that students benefit from the highly individualized instruction, the success of the program as well as the student is dependent on maximizing the demanding skills learned and applied during the course of instruction.

Therefore, students will be permitted no more than three instances of excessive tardiness prior to being subject to dismissal from the program. Excessive tardiness is defined as more than three instances during the course of instruction when the student is more than 15 minutes late at either the commencement of the class in the morning or in the afternoon.

Students will receive a warning and reminder of this policy after each of the first three instances of excessive tardiness. The Silicon Valley Polytechnic Institute, Inc. reserves the right to dismiss a student for excessive tardiness.

The instructor will determine what constitutes a valid excuse for tardiness. The general rule will be whether a reasonable person in similar circumstances would be in a position to arrive ready for instruction at the appointed time.

CANCELATION AND LEAVE OF ABSENCE POLICY

Student has the right to cancel the enrollment agreement and obtain a refund of charges paid through attendance at the first session of training, or the seventh day after enrollment, whichever is later. Students may initially request orally or in writing to drop out of the program or to receive a grant of a leave of absence for sufficient reasons as determined by the instructor. If such a request is communicated orally, it shall be requested in writing prior to approval by the instructor. This will be for the purpose of documenting the student record.

Re-admission to the program will be at the sole discretion and under conditions determined as appropriate and necessary by the instructor. The primary governing factor for re-admission will be the passage of time since the student was last in the program, and the instructor's estimate of student progress and capability, and the satisfaction of financial requirements.

Under no conditions will a student be permitted a leave of absence for more than a three-month period. If a student needs to discontinue the program of instruction for a period of more than three months, the student will receive a refund of paid tuition according to the refund policy and must thereafter be readmitted to the program.

Licensure is not required for these student graduates in order to work in the field and pursue their trade or vocation. SVPTI will not guarantee any employment or specific jobs upon completion of training. Instructors, in response to student questions, may offer general suggestions and references for locating employment in the field. However, SVPTI will make no representations about guaranteed or likely placement with an employer upon completion of any of its programs.

A very high percentage of students are typically already employed in the field in which they seek further training.

CANCELLATION, WITHDRAWALS AND REFUND

Student has the right to cancel the enrollment agreement, without any penalty or obligations, through attendance at the first class session or the seventh calendar day after enrollment, whichever is later.

After the end of the cancellation period, student has the right to stop school at any time; and has the right to receive a pro rata refund if the student has completed 60 percent or less of the scheduled days/hours in the current payment period in the program through the last day of attendance.

Cancellation may occur when the student provides a written notice of cancellation at the following address: 1754 Technology Drive, Suite 228, San Jose, CA 95110. This can be done by mail or by hand delivery.

The written notice of cancellation, if sent by mail, is effective when deposited in the mail properly addressed with proper postage. The written notice of cancellation need not take any particular form and however expressed, it is effective if it shows that the student no longer wishes to be bound by the Enrollment Agreement.

If the Enrollment Agreement is cancelled the school will refund the student any money he/she paid, less a registration or administration fee not to exceed $250.00, and less any deduction for equipment not returned in good condition, within 45 days after the notice of cancellation is received.

Please be advised that a constructive withdrawal of a student may also be made by the school. Such a withdrawal will be determined to have occurred if in the estimation of the school and instructor, the student has missed more than 4 training sessions without any excuse and/or notification.

Student may withdraw from the school at any time after the cancellation period (described above) and receive a pro rata refund if the student has completed 60 percent or less of the scheduled days/hours in the current payment period in your program through the last day of attendance. The refund will be less a registration or administration fee not to exceed $250.00, and less any deduction for equipment not returned in good condition, within 45 days of withdrawal. If the student has completed more than 60% of the period of attendance for which the student was charged, the tuition is considered earned and the student will receive no refund.

REFUND POLICY

For the purpose of determining a refund under this section, a student shall be deemed to have withdrawn from a program of instruction when any of the following occurs:

- The student notifies the institution of the student's withdrawal or as of the date of the student's withdrawal, whichever is later.
- The institution terminates the student's enrollment for failure to maintain satisfactory progress; failure to abide by the rules and regulations of the institution; absences in excess of maximum set forth by the institution; and/or failure to meet financial obligations to the School.
- The student has failed to attend class for three (3) consecutive weeks.
- The student fails to return from a leave of absence.

To determine the amount of the refund, the date of the student's withdrawal shall be deemed the last date of recorded attendance. The amount owed equals the daily charge for the program (total institutional charge, minus non-refundable fees, divided by the number of days/hours in the program), multiplied by the number of days/hours scheduled to attend, prior to withdrawal.

For the purpose of determining when the refund must be paid, the student shall be deemed to have withdrawn at the end of three (3) consecutive weeks. If the student has completed more than 60% of the period of attendance for which the student was charged, the tuition is considered earned and the student will receive no refund.

If any portion of the tuition was paid from the proceeds of a loan or third party, the refund shall be sent to the lender, third party or, if appropriate, to the state or federal agency that guaranteed or reinsured the loan. Any amount of the refund in excess of the unpaid balance of the loan shall be first used to repay any student financial aid programs from which the student received benefits, in proportion to the amount of the benefits received, and any remaining amount shall be paid to the student. If the student has received federal student financial aid funds, the student is entitled to a refund of moneys not paid from federal student financial aid program funds.

FEDERAL OR STATE LOANS:

Silicon Valley Polytechnic Institute, Inc. does not participate in any state and federal financial aid programs.

NOTICE CONCERNING TRANSFERABILITY OF CREDITS AND CREDENTIALS EARNED AT OUR INSTITUTION

The transferability of credits you earn at Silicon Valley Polytechnic Institute, Inc. is at the complete discretion of an institution to which you may seek to transfer. Acceptance of the certificate that you earn in Silicon Valley Polytechnic Institute, Inc. is also at the complete discretion of the institution to which you may seek to transfer. If the certificate that you earn at this institution is not accepted at the institution to which you seek to transfer, you may be required to repeat some or all of your coursework at that institution.

For this reason, you should make certain that your attendance at this institution will meet your educational goals. This may include contacting an institution to which you may seek to transfer after attending Silicon Valley Polytechnic Institute, Inc. to determine if your certificate will transfer.

Prior to signing an enrollment agreement, you must be given a catalog or brochure and a School Performance Fact Sheet, which you are encouraged to review prior to signing this agreement. These documents contain important policies and performance data for this institution. This institution is required to have you sign and date the information included in the School Performance Fact Sheet relating to completion rates, placement rates, license examination passage rates, and salaries or wages, prior to signing this agreement.

PROBATION AND DISMISSAL

Silicon Valley Polytechnic Institute, Inc. reserves the right to suspend or terminate any student whose conduct is deemed inappropriate and disruptive to instruction. Students will be expected to fully observe policies and rules of conduct of the Silicon Valley Polytechnic Institute, Inc. Such conduct includes: excessive absences or tardiness; failure to maintain satisfactory progress; inappropriate behavior toward another student or staff member; failure to abide by school rules and regulations; failure to meet financial obligations; any other conduct deemed sufficiently disruptive of instruction so that, in the estimation of the instructor and CEO/President, continued instruction is not a reasonable or constructive proposition.

Students who have been suspended or terminated may request reinstatement in writing to the President after a period of at least thirty days. Decisions on reinstatement will be at the sole discretion of Silicon Valley Polytechnic Institute, Inc.

TOTAL CHARGES TO BE PAID UPON ENROLLMENT:

Tuition	Please see appendix II
Registration Fee	$150 (Also see appendix II)
STRF Fee	**
Leave of Absence Fee	N/A
Textbooks or Materials Charges	Student is responsible for purchasing necessary textbooks. Estimated charges:

**Effective April 1, 2022, the Student Tuition Recovery Fund (STRF) assessment rate is two dollars and fifty cents ($2.50) per one thousand dollars ($1,000) of institutional charges. See page 15 for STRF description.

The student will be responsible for these amounts. If the student has a student loan, they will be responsible for repaying the loan amount plus any interest, less the amount of any determined refund.

STUDENT TUITION RECOVERY FUND (STRF) FEES:

The State of California established the Student Tuition Recovery Fund (STRF) to relieve or mitigate economic loss suffered by a student in an educational program at a qualifying institution, who is or was a California resident while enrolled, or was enrolled in a residency program, if the student enrolled in the institution, prepaid tuition, and suffered an economic loss. Unless relieved of the obligation to do so, you must pay the state-imposed assessment for the STRF, or it must be paid on your behalf, if you are a student in an educational program, who is a California resident, or are enrolled in a residency program, and prepay all or part of your tuition.

You are not eligible for protection from the STRF and you are not required to pay the STRF assessment, if you are not a California resident, or are not enrolled in a residency program.

It is important that you keep copies of your enrollment agreement, financial aid documents, receipts, or any other information that documents the amount paid to the school. Questions regarding the STRF may be directed to the Bureau for Private Postsecondary Education, 1747 North Market Blvd., Suite 225, Sacramento, California, 95834, (916) 574-8900 or (888) 370-7589.

To be eligible for STRF, you must be a California resident or enrolled in a residency program, prepaid tuition, paid or deemed to have paid the STRF assessment, and suffered an economic loss as a result of any of the following:

1.The institution, a location of the institution, or an educational program offered by the institution was closed or discontinued, and you did not choose to participate in a teach-out plan approved by the Bureau or did not complete a chosen teach-out plan approved by the Bureau.

2.You were enrolled at an institution or a location of the institution within the 120 day period before the closure of the institution or location of the institution, or were enrolled in an educational program within the 120 day period before the program was discontinued.

3.You were enrolled at an institution or a location of the institution more than 120 days before the closure of the institution or location of the institution, in an educational program offered by the institution as to which the Bureau determined there was a significant decline in the quality or value of the program more than 120 days before closure.

4.The institution has been ordered to pay a refund by the Bureau but has failed to do so.
5.The institution has failed to pay or reimburse loan proceeds under a federal student loan program as required by law or has failed to pay or reimburse proceeds received by the institution in excess of tuition and other costs.

6.You have been awarded restitution, a refund, or other monetary award by an arbitrator or court, based on a violation of this chapter by an institution or representative of an institution, but have been unable to collect the award from the institution.

7.You sought legal counsel that resulted in the cancellation of one or more of your student loans and have an invoice for services rendered and evidence of the cancellation of the student loan or loans.

To qualify for STRF reimbursement, the application must be received within four (4) years from the date of the action or event that made the student eligible for recovery from STRF.

A student whose loan is revived by a loan holder or debt collector after a period of noncollection may, at any time, file a written application for recovery from STRF for the debt that would have otherwise been eligible for recovery. If it has been more than four (4) years since the action or event that made the student eligible, the student must have filed a written application for recovery within the original four (4) year period, unless the period has been extended by another act of law.

However, no claim can be paid to any student without a social security number or a taxpayer identification number."

STUDENT LOANS

If a student has a student loan, they are responsible for repaying the loan amount plus any interest, less the amount of any determined refund. If a student has received federal student financial aid funds, the student is entitled to a refund of the moneys not paid from federal student financial aid program funds.

BANKRUPTCY

The State of California requires that we inform students that Silicon Valley Polytechnic Institute, Inc. does not have a pending petition in bankruptcy, is not operating as a debtor in possession, nor has filed a petition within the preceding five years that resulted in reorganization under Chapter 11 of the United States Bankruptcy Code.

PLACEMENT SERVICES

SVPTI does not guarantee employment or any specific job upon completion of training. Instructors, in response to student questions, may offer general suggestions and references for locating employment in the field. However, SVPTI will make no representations about guaranteed or likely placement with an employer upon completion of any of its programs.

A very high percentage of students are typically already employed in the field in which they seek further training.

FACILITIES AND EQUIPMENT

SVPTI training programs are class room based and students do not need any specific equipment. We will use computers, projectors, and white boards.

The proposed programs for SVPTI will be provided at its main location. SVPTI is located at 1754 Technology Drive, Suite 228, San Jose, CA 95110. The school premises are located on the second floor of a two-story building in an office complex with ample parking.

The institution's floor plan includes two classrooms, with the remaining space primarily shared between offices, a reception area, and administrative support functions, a conference room and library area, and kitchen facility. Restroom facilities are located in two nearby locations, adjacent to Suite 228. Library is accessible to all students without any formal procedure.

SVPTI is located in a pleasant office park with similar two-story buildings and a diversity of businesses appropriate to an office park. The overall appearance of the facility is that it is perhaps 10 to 15 years old with mature trees and landscaping. Offices and classrooms have plenty of windows. Rooms are ample in size. The facility is well-maintained and has an atmosphere conducive to learning.

LIBRARY AND INFORMATION RESOURCES

All students are provided with the program or course text and software at no extra charge.

Students also have access to the Internet for any reference purpose through the various computers on-site.

Students do have access to an on-site reference library. Students can borrow on-site library books by sending email to info@svpti.com with the name of the book and duration it is needed. If requested, students will be provided with a letter of introduction by SVPTI for access to any other library facilities. However, between what is provided to students by SVPTI in terms of texts and software, and their access to the Internet, this is really all that is necessary for this type of instruction.

The proposed instruction will be provided with a very low ratio of instructors to students. Over the course of this type of instruction there is ample opportunity, actually much more opportunity than is typically the case, for direct exchange between the instructor and the student. A wealth of information is provided in this manner.

The library resources as described above are more than sufficient to support the instructional needs of anticipated or projected students.

Office of Student Assistance and Relief

The Office of Student Assistance and Relief is available to support prospective students, current students, or past students of private postsecondary educational institutions in making informed decisions, understanding their rights, and navigating available services and relief options. The office may be reached by calling Toll-free telephone #: (888) 370-7589 or by visiting www.osar.bppe.ca.gov.

STUDENT SERVICES

Though Silicon Valley Polytechnic Institute, Inc. does not provide actual tutorials, the training provided has a very favorable instructor-to-student ratio, thereby facilitating instruction and learning for students. Though this teaching method is not by itself considered to constitute a traditional "student service," as a practical matter, it is far more valuable to the individual student than many other more traditional student services.

There is a considerable amount of “academic counseling” built into this program. Because the nature of the instruction is relatively intimate and direct, students will inevitably glean a considerable amount of practical and useful information from the instructor during the training, especially, of course, in the practical instructional phase.

Silicon Valley Polytechnic Institute, Inc. carefully balances and integrates theory with practical content and processes in order to considerably shorten the student’s learning curve.

With the exception of required textbooks and writing materials, any required materials or equipment for practicum or other instruction are provided by the Silicon Valley Polytechnic Institute, Inc. and paid for as part of the tuition.

Academic counseling is provided by or through instructors as well as the CEO/President on occasion.

There is a student lounge area with a refrigerator and microwave. Students may use this area to lunch, rest, or study.

A small library or reference area is provided. Some copies of texts as well as industry trade journals and magazines are available for browsing.

The above items are for student use during normal school hours only. There will be no lending library.

There is plenty of parking immediately adjacent to the building.

Silicon Valley Polytechnic Institute, Inc. is conveniently accessible off a main thoroughfare and near a major freeway. A variety of retail services are available nearby.

NEARBY HOUSING

Silicon Valley Polytechnic Institute, Inc. has no dormitory facilities. The availability of housing nearby varies greatly in price and lease terms. The estimation of the approximate cost of the housing in the neighborhood is about $1000 to $2,000 per month, depending on each student’s needs.
Silicon Valley Polytechnic Institute, Inc. has no responsibility to find or assist students with their housing needs. This is the sole responsibility of the student.

STUDENT VISAS

Silicon Valley Polytechnic Institute, Inc. does not admit students with student visas from other countries.

SCHOOL FINANCIAL AID

There is no private financing available through the school. Students are advised to obtain financial aid from a financial institution. Students at SVPTI are typically able to pay for a course of instruction upon enrollment.

DISTANCE EDUCATION

No part of the required instruction taken through Silicon Valley Polytechnic Institute, Inc. may be acquired via distance learning. Of course, some of the instruction may be supplemented via distance learning methods.

STUDENT RIGHTS AND GRIEVANCES

Students at Silicon Valley Polytechnic Institute, Inc. enjoy all the rights and privileges mentioned elsewhere in this catalog, including the right to cancel or withdraw, the right to a reasonable refund in such circumstances, and the privileges associated with being a student at the school.

However, it is recognized that, even with a favorable ratio of instructors to students, a dispute may arise with respect to the instruction or a school policy or practice that a student perceives as unfair or damaging.

A student may lodge a complaint orally or in writing to the instructor at the address of the school. The instructor, upon receipt of a complaint, will attempt to resolve the issue(s) directly with the student.

If the student complaint is not resolved within a reasonable period of time, for example within three to five days, or prior to the need for the student to lodge the complaint again, the instructor will advise the student that the complaint must be provided in writing if it hasn't been already. At that point, the instructor will provide the student with a written summary of the official complaint policy, as described in this catalog.

If a student complains in writing, the Silicon Valley Polytechnic Institute, Inc. will provide the student with a written response within ten days of receipt of the student complaint. The written response will include a summary of the school investigation and disposition of the complaint. If the complaint or relief requested by the student is rejected, specific reasons will be given for the rejection.

If the student remains dissatisfied with the rejection or proposed remedy provided by the school, they may resort to contacting the Bureau at the address provided on their enrollment agreement or take other appropriate action as dictated by the circumstances.

STUDENT RECORDS

SVPTI will maintain a file for each student who enrolls in the institution regardless of whether the student completes the educational service.

As set forth in California Education Code (CEC) §94900, Silicon Valley Polytechnic Institute, Inc. (SVPTI) will maintain records with the name and most current address, e-mail address, and telephone number of each student enrolled in an educational program at the institution. Course and faculty information will be maintained as a matter of record for a period of not less than five years, and will contain the following information:

- Complete and accurate records of the educational programs offered and the curriculum for each
- The names and addresses of the members of the faculty, and
- Records of the educational qualifications of each member of the faculty.

In addition to the requirements of CEC Section 94900, the file shall contain all of the following applicable information per CCR Section 71920:

- Written records and transcripts of any formal education or training, testing, or experience that are relevant to the student's qualifications for admission to the institution or the institution's award of credit or acceptance of transfer credits including the following:

  (A) Evidence of high school completion or equivalency or other documentation establishing the student's ability to do college level work;

  (B) Records documenting units of credit earned at other institutions that have been accepted and applied by the institution as transfer credits toward the student's completion of an educational program;

  (C) Grades or findings from any examination of academic ability or educational achievement used for admission or college placement purposes;

  (D) All of the documents evidencing a student's prior experiential learning upon which the institution and the faculty base the award of any credit;

  Please note that since SVPTI does not offer any credit for student's prior experiential learning and they will not be considered as a basis for acceptance and/or granting the certificate.

- Personal information regarding a student's age, gender, and ethnicity if that information has been voluntarily supplied by the student;
- Copies of all documents signed by the student, including contracts, instruments of indebtedness, and documents relating to financial aid;
- Records of the dates of enrollment and, if applicable, withdrawal from the institution, leaves of absence, and graduation; and
- A transcript showing all of the following:

  (A) The classes and courses or other educational programs that were completed, or were attempted but not completed, and the dates of completion or withdrawal;

  (B) The final grades or evaluations given to the student;

  (C) Credit awarded for prior experiential learning, including the course title for which credit was awarded and the amount of credit (Please note this does not apply to SVPTI since as mentioned above, SVPTI will not consider student's prior experiential learning as a basis for acceptance and/or granting the certificate);

  (D) Credit for courses earned at other institutions;

  (E) Credit based on any examination of academic ability or educational achievement used for admission or college placement purposes;

  (F) Degrees and diplomas awarded the student; and

  (G) The name, address, email address, and telephone number of the institution.

- For independent study courses, course outlines or learning contracts signed by the faculty and administrators who approved the course;

- The dissertations, theses, and other student projects submitted by graduate students;
- A copy of documents relating to student financial aid that are required to be maintained by law or by a loan guarantee agency;
- A document showing the total amount of money received from or on behalf of the student and the date or dates on which the money was received;
- A document specifying the amount of a refund, including the amount refunded for tuition and the amount for other itemized charges, the method of calculating the refund, the date the refund was made, and the name and address of the person or entity to which the refund was sent;
- Copies of any official advisory notices or warnings regarding the student's progress; and
- Complaints received from the student.

SVPTI will also keep the following documentation in the student record:

- The application for admission
- The notice or letter of acceptance or admission to the Institute
- Any documentation regarding cancellation, withdrawal, leave of absence, refund, or correspondence regarding a disciplinary action
- The title of the certificate granted to the student
- The date the certificate was granted
- The courses and units upon which the certificate was based (transcript)
- The grades earned in each course by the student (transcript)
- Any documentation regarding graduation
- Any correspondence regarding a student complaint
- Any calculation of a refund amount due to the student
- Any correspondence regarding any of the above.

Financial records will generally be maintained separate from academic documentation. These records will be maintained as hard copies and also easily accessible and downloadable for the review of any authorized institutional officer or regulating authority.

All student records will be maintained in California. All student transcripts and other records will be maintained permanently.

Finally, after a sufficient period of operation, and as required, SVPTI will maintain on-site for a period of not less than five years all data and records regarding completion, placement, licensure (if applicable), and salary disclosure requirements for graduates who find employment in the field within the guidelines prescribed in California Education Code Section 94928.

OCCUPATIONS OR JOB TITLES

Silicon Valley Polytechnic Institute, Inc. will not guarantee any employment or specific jobs upon completion of training. Instructors, in response to student questions, may offer general suggestions and references for locating employment in the field. However, Silicon Valley Polytechnic Institute, Inc. will make no representations about guaranteed or likely placement with an employer upon completion of any of its programs.

A significant percentage of students may already be employed in some capacity in the field in which they seek further training.

There will be no formalized placement office at Silicon Valley Polytechnic Institute, Inc.. But it is expected that Silicon Valley Polytechnic Institute, Inc. will, especially as its reputation grows, have a considerable network of contacts within the local and regional business community and its particular business sector. Due to the nature of the instruction and the relatively close-knit community of a small to medium size school, it is further expected that fellow students, instructors, as well as school officials will be able to meaningfully assist students in their search for and ability to obtain employment in the sector.

Proximity to the populous counties of the Bay Area, of which Silicon Valley Polytechnic Institute, Inc. will be a part, will materially assist these endeavors. However, it is important to remember that there are no specific occupations or job guarantees or promises of placement made upon graduation from a Silicon Valley Polytechnic Institute, Inc. course or program.

Sample SOC Codes for typical job classifications available to graduates are as follows:

17-3011	Civil Computer-Aided Design and Drafting Technicians
17-3011	Civil Drafters
17-3012	Electrical and Electronics Drafters
15-1132	Computer Applications Engineers
51-4010	Computer Control Programmers and Operators
17-2061	Computer Hardware Designers
17-2061	Computer Hardware Developers
17-2060	Computer Hardware Engineers
17-2061	Computer Hardware Engineers
15-1131	Computer Programmers
49-2011	Computer Repairers
47-2111	Solar PV Electricians
47-2231	Solar PV Installers
47-2111	Solar Photovoltaic Electricians
47-2230	Solar Photovoltaic Installers
47-2231	Solar Photovoltaic Installers
17-3012	Technicians, Electrical Computer-Aided Design and Drafting
17-3023	Technicians, Electrical Design
17-3023	Technicians, Electrical Engineering
17-3024	Technicians, Electro-Mechanical
17-3023	Technicians, Electronics Engineering
13-1082	Project Management Specialists

Appendix-III shows the SOCO codes for all programs offered by Silicon Valley Polytechnic Institute, Inc.
SVPTI prides itself on the attention and instruction provided to students. Students will obtain an understanding and appreciation for both the theory and practical knowledge of the subjects covered. You will find your pursuit of training at SVPTI enhanced by instructors who care and have direct experience with what they teach. And you will find that instruction supplemented by a learning environment conducive to obtaining what you need.

APPENDIX –I

This appendix provides the outline of all training programs offered by Silicon Valley Polytechnic Institute, Inc. (SVPTI). Unless otherwise stated, the following applies to all training programs shown:

1. None of the programs require internship/externship.
2. Each training program includes a midterm exam, final exam, quizzes and project assignments. Grades will be based on predominantly objective criteria such as exam results, projects, presentations, maintaining attendance, participation in class and engagement with the material.
3. Silicon Valley Polytechnic Institute, Inc. (SVPTI) will assess and evaluate student performance in order to grant a certificate of completion.
4. SVPTI will require that a student earn at least a C average (2 points on a 4 points scale) in order to satisfactorily complete a course of instruction.

a) Course Title:

Computer Aided Design and Drafting with AutoCAD (CAD-100)

b) Objectives:
AutoCAD Design and Drafting for Professionals provides students with extensive hands-on experience with the latest AutoCAD software, which is the world's leading CAD software for design & drafting. Participants will work with advanced drafting methods, as well as powerful AutoCAD features with exmaples in various aspects of design exploration for architectural, civil, mechanical, and electrical applications.

d) Length of program:
The course duration is 12 weeks.

e) Class Sessions
Classes are being held twice a week, with each session typically 3 hours long.

f) Text Books
AutoCAD 2011, A Problem Solving Approach, Sham Tickoo, autodesk Press.

g) Course Outline

- Why use 3D Surfaces vs. Solids
- Surfaces and Solids
- Creating surfaces
- Lines, arcs and circles with thickness
- 3D Faces
- 3D Mesh
- Creating solids
- Primitives
- Extrude
- Revolve
- Editing surfaces, solids
- Spherical & Cylindrical coordinate systems
- Co-ordinate Systems, Editing Tools
- World Co-ordinate System
- UCSICON
- UCS - how to set up efficiently
- Display Commands - dview, ddvpoint, plan, vpoint
- 3D Drawing and Editing Commands. Primitives
- Model Space/Paper Space
- Editing viewports
- Placing rendered images in a viewport
- Visualization Techniques
- Rendering Concepts
- Adding Materials to the Model
- Scenes and Lighting
- Adding Bitmap Images
- Class Exercises and projects

h) Education Requirements
High School or higher

i) Course Level
Entry Level, Technician

j) Method of Instruction
On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Advanced and 3D Computer Drafting and Design with AutoCAD (CAD-120)

b) Objectives:

This course introduces students to the process, tools, and methodology of computer drafting with AutoCAD, the world's leading CAD software for design & drafting. This multipurpose class is intended for those who have little or no experience with AutoCAD. During the course, students will acquire basic skills in the use of AutoCAD software and design techniques toward various applications.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, with each session typically 3 hours long.

f) Text Books

AutoCAD 2010, A Problem Solving Approach, Sham Tickoo, autodesk Press.

g) Course Outline

- Getting Started with AutoCAD
- Basic Drawing and Editing Commands
- Drawing Organization and Information
- Organizing Your Drawing with Layers
- Advanced Editing Commands
- Inserting Blocks
- Printing
- Annotating
- Adding Text
- Hatching
- Adding Dimensions
- Advanced Editing Features
- Changing an Object's Length
- Productivity Tools
- Efficient Construction Techniques
- Accurate Positioning
- Creating and Managing Blocks
- Drawing Setup and Utilities
- Creating Templates
- Advanced Viewing Tools
- Quick Editing Techniques
- Viewing What You Need
- Advanced Object Types
- Polylines and Regions
- Multilines
- Advanced Blocks and Attributes
- Referencing and Sharing Information
- External Reference
- Working with Images
- Layouts and Plotting
- Working with Layouts
- Drawing Standards and System Setup
- Maintaining Standards
- CAD Standards
- Introduction to Customization

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Technician

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Mechanical Drafting Fundamentals (CAD-130)

b) Objectives:

This course introduces fundamental concepts and operations necessary to utilize personal computer for developing fundamental drafting techniques. Emphasis is placed on the basic concepts, geometric terms/media sizes, and techniques necessary for CAD applications. Topics include history of drafting, safety practices, terminology, hardware and software care and use, basic entities, CAD commands, line relationships, basic CAD applications, and geometric construction.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, with each session typically 3 hours long.

f) Text Books

The Art of Mechanical Drawing: A Practical Course for Drafting and Design
William F. Willard

g) Course Outline

- Describe the role of technical graphics in the engineering design process.
- Produce multi-view orthographic views.
- Create sectional views.
- Create auxiliary views.
- Scale drawings.
- Apply dimensions to drawings.
- Create pictorial drawings.
- Prepare development drawings.
- Identify graphics for fastening and finishing machine components.

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Technician

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Computer Aided Design and Drafting with SolidWorks (CAD-140)

b) Objectives:

This course introduces the students to the process, tools, and methodology of 3D computer drafting with SolidWorks, the world's leading CAD software for 3D design & drafting and modeling. During the course, the students will acquire skills in the use of SolidWorks software and design techniques for design and drawing of various 3D structures for many diverse applications. This course prepares students for entry-level to mid-level positions in the industry.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, with each session typically 3 hours long.

f) Text Books

SolidWorks 2010 for Designers, By Sham Tickoo, Purdue University, ISBN: 1-932709-26-6

g) Course Outline

- Why use 3D Surfaces vs. Solids
- Surfaces and Solids
- Creating surfaces
- Lines, arcs and circles with thickness
- 3D Faces
- 3D Mesh
- Creating solids
- Primitives
- Extrude
- Revolve
- Editing surfaces, solids
- Spherical & Cylindrical coordinate systems
- Co-ordinate Systems, Editing Tools
- World Co-ordinate System
- UCSICON
- UCS - how to set up efficiently
- Display Commands - dview, ddvpoint, plan, vpoint
- 3D Drawing and Editing Commands. Primitives
- Model Space/Paper Space
- Editing viewports
- Placing rendered images in a viewport
- Visualization Techniques
- Rendering Concepts
- Adding Materials to the Model
- Scenes and Lighting
- Adding Bitmap Images
- Class Exercises and projects

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Technician

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Advanced 3D Computer Aided Design and Drafting with SolidWorks (CAD-160)

b) Objectives:

This course introduces the students to the advanced modeling techniques using SolidWorks, the authoritarian in 3D Mechanical Computer Aided Design (MCAD). This multipurpose class is designed for students that have completed the introductory class to SolidWorks, or individuals with industry experience looking to expand their knowledge with SolidWorks. Thru various examples, students will utilize SolidWorks software to learn advanced design techniques geared toward mechanical, structural, and architectural applications. This course prepares students for mid-level to advanced-level positions in the industry.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, with each session typically 3 hours long.

f) Text Books

SolidWorks 2010 for Designers, By Sham Tickoo, Purdue University, ISBN: 1-932709-26-6

g) Course Outline

- Advanced sketching techniques
- 3D Sketching
- Auto dimension
- Contrain all/find equal
- 2D to 3D Tools
- Sweeps and Lofts
- Surfacing Tools
- Sheet metal Tools
- Design Library
- Troubleshooting parts (fixing rebuild errors)
- Disjoint bodies/multibody part modeling
- Weldment Tools
- Configurations & Design Tables
- Importing/Exporting files
- Advanced assembly techniques
- Advanced mates
- Assembly level features
- Patterns and mirrors
- Flexible Assemblies
- Top Down Assembly modeling
- Layout Sketches
- Collision Detection and Physical Dynamics
- Large Assembly modeling techniques
- Assembly Configurations & Design Tables

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Technician

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Autodesk Revit Architecture Essentials (CAD-180)

b) Objectives:

This course introduces the students to the process, tools, and methodology of using Autodesk Revit for architectural drafting. This course is intended for those who have already taken the AutoCAD or are fairly familiar with AutoCAD. During the course, the students will acquire skills in the use of Revit software and design techniques for various architectural applications.

d) Length of program:

The course duration is 12 weeks long.

e) Class Sessions

Classes are being held twice a week, with each session typically 3 hours long.

f) Text Books

Mastering Autodesk Revit Architecture 2011, By Eddy Krygiel*, et al*
ISBN-10: 0470626968

g) Course Outline

- What Is Revit Architecture?
- Overview of the Revit Architecture Interface
- Revit Architecture File Types
- Creating Basic Floor Plans
- General Drawing and Sketch Tools
- Drawing Walls
- Adding Doors and Windows
- Setting Up Levels and Grids
- Creating and Using Levels
- Creating Structural Grids and Columns
- Modifying Specific Objects
- Selecting & Modifying Objects
- Modifying Walls
- Modifying Levels
- Modifying Doors and Windows
- Modifying Structural Grids and Columns
- Editing Commands
- Moving and Copying Objects
- Rotating Objects
- Resizing Objects
- Creating Linear and Radial Arrays
- Mirroring Objects
- Aligning Objects
- Splitting Walls and Lines
- Offsetting Objects
- Trimming and Extending
- Creating Views of the Model
- Using the Project Browser
- Working with Views
- Setting Up Views
- Viewing Elevations
- Cutting Sections
- Creating Callouts
- Duplicating Views
- Creating 3D Views
- Adding Components
- Loading Families from Libraries
- Manipulating Components
- Floors and Ceilings
- Creating Floors
- Creating Ceilings
- Creating Roofs
- Creating Roofs by Extrusion
- Stairs, Railings, and Ramps
- Creating Stairs
- Adding and Modifying Railings
- Creating Ramps
- Curtain Walls
- Creating Curtain Walls
- Creating Curtain Wall Types with Automatic
- Working with Curtain Wall Panels
- Attaching Mullions to Curtain Grids
- Sheets and Printing
- Setting Up Sheets
- Views and Sheets
- Printing Sheets
- Annotation
- Working With Text
- Adding Dimensions
- Adding Tags
- Building Schedules
- Detailing in Revit Architecture
- Setting Up Detail Views
- Creating Details
- Annotating Details
- Revision Tracking
- Creating Legen

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Technician

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Computer and Network Security Essentials (CIE-150)

b) Objectives:

This course introduces the students to Principles, mechanisms and implementation of computer security and data protection. Policy, encryption and authentication, access control and integrity models and mechanisms; network security; secure systems; programming and vulnerabilities analysis. The course will also include study of existing operating systems. This course prepares students for entry-level to mid-level positions in the industry.

d) Length of program:

The course duration is 12 weeks long.

e) Class Sessions

Classes are being held twice a week, with each session typically 3 hours long.

f) Text Books

Network Security Bible, By Eric Cole, ISBN: 0764573977

g) Course Outline

- What is computer security: notion of an informal policy, formalization of policy
- Encryption: classical, public-key; implementation, problems; the Linux file encryption mechanism and its cryptanalysis; the DES and RSA
- Authentication: model of authentication systems, traditional passwords, challenge/response, one-time passwords; cryptographic protocols, simple cryptosystems; the standard Linux authentication system, its limits and alternate forms; implementations of other mechanisms
- Access control: controlling access to resources, access matrix model, undecidability result, access control lists and capability lists; mandatory controls, originator controls; variants; Linux scheme and augmentations
- Integrity: cryptographic checksums, malicious logic, viruses, Trojan horses; defenses, prevention; Linus integrity checking tools and how they work; malicious logic and Linux
- Security-oriented programming: design principles, focusing on common problems; gates vs. privileged servers; environment, exception handling; writing secure servers and secure setuid/setgid programs in the Linux environment
- Networks and security: Internet Security Architecture, analysis of Internet protocols, design and implementation considerations; firewalls; Linux networking and security
- Penetration analysis: common types of flaws, examples, flaw hypothesis methodology, analysis of programs and systems; Linux instances of problems, flaws, and how to fix them
- Secure systems: types, models, design, changes to non-secure systems; comparative analysis

h) Education Requirements

AA or higher

i) Course Level

Entry Level, Technician, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 72 hours of lecture and 48 hours of computer Lab

a) Course Title:

Software Quality Assurance Essentials (CS-150)

b) Objectives:

This course focuses on techniques for ensuring software quality. In this course quality assurance is viewed as a holistic activity that runs through the entire development process: understanding the needs of clients and users; analyzing and documenting requirements; verifying and validating solutions through testing.

d) Length of program:

The course duration is 12 weeks long.

e) Class Sessions

Classes are being held twice a week, with each session typically 3 hours long.

f) Text Books

Software Quality Assurance, By D. Galin
ISBN 978-0-201-70945-2

g) Course Outline

- Evaluating usability of a software product.
- Requirements analysis. Software development as problem solving.
- Identifying, structuring, and classifying problems through Problem Frames.
- Building specifications from requirements.
- Verification and validation. Defining the testing mission. Test strategies.
- Techniques of conformance testing.
- Validating preliminary designs through prototyping.
- Quality management. Measuring software quality.
- Software quality standards.

h) Education Requirements
AA or higher

i) Course Level
Entry Level, Technician, Engineering

j) Method of Instruction
On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Solar Photovoltaic System Design Essentials (EN-100)

b) Objectives:

This course provides the students with a comprehensive understanding of Photovoltaic (PV) Solar systems. The class covers essentials of PV theory, design, configuration and installation techniques and employs a balanced combination of lecture and hands-on practice. The course is intended for contractors, installation consultants, and electricians new to the solar industry, and is intended to prepare participants for employment in renewable energy industry. This course prepares students for entry-level to mid-level positions in the industry.

d) Length of program:

The course duration is 12 weeks long.

e) Class Sessions

Classes are being held twice a week, with each session typically 3 hours long.

f) Text Books

Photovoltaic Systems, ATP Publications, ISBN 978-0-8269-1287-9

g) Course Outline

- Photovoltaics, photovoltaic (PV) system, and load.
- Advantages of using PV systems.
- Disadvantages of using PV systems.
- Process of electricity distribution.
- Development of PV technology.
- Common applications of PV systems.
- Common methods of converting solar radiation into heat energy.
- How solar energy can be harnessed through chemical processes.
- Characteristics and advantages of solar lighting.
- Solar radiation, solar irradiance, and the inverse square law.
- Solar irradiation.
- Solar constant and the solar spectrum in relation to extraterrestrial solar radiation.
- Characteristics of direct radiation and diffuse radiation.
- Various stages of Earth's orbit.
- Characteristics of solar time as contrasted with standard time.
- Various positions of the sun.
- Ways that array orientation can vary due to geographical and seasonal variations of the sun's path.
- Function of solar radiation data sets and which agencies provide the data.
- Customer concerns and site issues that may arise during a preliminary assessment.
  Common types of equipment needed to conduct site surveys.
- Features of the profile angle shading analysis method and the photographic method.
- Main reasons to consider accessibility when conducting a site survey.
- Factors to consider when evaluating roofs.
- Conducting an electrical assessment.
- Energy audit and opportunities for conservation and energy efficiency.
- Preparing a proposal.
- Major components of PV systems
- Common sources of electricity.
- Utility-interactive system and common metering arrangements.
- Advantages and classifications of hybrid systems.
- Basic composition and use of PV cells.
- Photovoltaic effect and the fundamentals of PV cells.
- Common PV cell materials.
- Advantages and disadvantages of different silicon wafers.
- Process of cell fabrication.
- How a PV device responds to changes in solar irradiance and temperature.
- Basic function and construction of modules and arrays.
- Function and main features of bypass diodes.
- Common module and array standards and performance ratings.
- Main principles and components of battery design.
- Steady-state and capacity.

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Technician

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Advanced Solar Photovoltaic System Design (EN-120)

b) Objectives:
This course provides the students with advanced topics in Photovoltaic (PV) Solar systems. The course is intended for contractors, installation consultants, and electricians new to the solar industry, and is intended to prepare participants for employment in renewable energy industry. This course prepares students for entry-level to mid-level positions in the industry.

d) Length of program:
The course duration is 12 weeks long.

e) Class Sessions
Classes are being held twice a week, with each session typically 3 hours long.

f) Text Books
Photovoltaic Systems, ATP Publications
ISBN 978-0-8269-1287-9

g) Course Outline

- Distributed generation and function of generators in an electric utility system.
- How inverters differ from generators.
- Main advantages of bimodal systems.
- Requirements associated with different points of connection.
- Compare and contrast the main methods of metering electricity.
- How legislation has impacted the adoption of PV and other distributed-power systems.
- Main procedural steps necessary for getting approval for an interconnection agreement.
- Common requirements of utility interconnection agreements.
- Role of building codes in electrical installations.
- Issues related to electrical contractor licensing.
- Building regulations that may restrict or facilitate construction
- Minimum requirements for most permit applications.
- Roles of permit fees and the plans review as requirements for permit issuance.
- Documentation commonly used during the inspection process.
- Common items included on an inspection check.
  Advantages and limitations of an inspection check.
- Steps involved in commissioning a new PV system.
- Maintenance tasks for arrays.
- Tasks and tools related to battery maintenance.
- Tasks performed for electrical equipment maintenance.
- Function of maintenance plans and maintenance logs.
  Steps involved in troubleshooting PV systems

h) Education Requirements
High School or higher

i) Course Level
Entry Level, Technician

j) Method of Instruction
On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*
Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Advanced Semiconductor Devices - Physics & TCAD (SS-200)

b) Objectives:

This course introduces students to the physics, operations and applications of semiconductor devices such as PN and Schottky diodes, bipolar and CMOS transistors. TCAD software is used when necessary to enhance the learning experience.

d) Length of program:

The course duration is 12 weeks long.

e) Class Sessions

Classes are being held twice a week, with each session typically 3 hours long.

f) Text Books

Physics of Semiconductor Devices by S.M.Sze, Wiley Publication
SBN 471 84290 7

g) Course Outline

- Semiconductor Materials & Atomic Models
- Energy Bands and Charge Carriers
- Bond and Band Models
- Carrier Concentrations
- Drift and Diffusion
- Continuity Equations
- PN Juncti ons Chapter
- Abrupt Junction
- Linearly Graded Junction
- Continuity Equations
- Generation and Recombination
- I-V Characteristics
- Bipolar Transistor
- Ebers-Moll Model
- Second Order Effects
- MOS Structure
- Flat Band Model
- Non-Flat Band Model
- Interface Charge Effects
- MOS Field Effect Transistors
- MOSFET Parameters

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Solar Photovoltaic Device Physics (SS-210)

b) Objectives:

This course provides the students with a comprehensive understanding of the physics of solar cell. Course starts with a description of property of semiconducting materials such as Si, and GaAs and then gives a detail description of the physics of PN junction as related to PV. TCAD software is used extensively to enhance the student's learning experience. This course prepares students for entry-level to mid-level positions in the industry.

d) Length of program:

The course duration is 12 weeks long.

e) Class Sessions

Classes are being held twice a week, with each session typically 3 hours long.

f) Text Books

The Physics of Solar Cells, by Jenny Nelson
ISBN 1860943497

g) Course Outline

- Introduction to solar cells
- Brief comparison with other renewables
- Properties of sunlight
- p-n junction physics; operation of solar cells
- Cell characterization: I-V curve under dark and illumination conditions,
- cell efficiency, fill factor, short-circuit current, open-
- circuit voltage
- PV technologies:
- Single crystalline Si cells
- Micro-, poly-, and multi-crystalline Si cells
- Amorphous Si cells
- III-V multijunction cells
- Concentrator PV
- CIGS solar cells
- CdTe solar cells
- Dye-sensitized solar cells
- Organic solar cells
- Nanotechnology and solar cells
- Module manufacturing
- PV Economics

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Advanced Semiconductor Technology and Fabrication (SS-220)

b) Objectives:

This course introduces students to the technology and manufacturing of silicon microchips. Course starts with an overview of semiconductor technology and proceeds to offer a detail description of all the process steps and equipments for making the modern semiconductor devices/products. The course will also provide an overview description of the latest advancements in semiconductor technology.

d) Length of program:

The course duration is 12 weeks long.

e) Class Sessions

Classes are being held twice a week, with each session typically 3 hours long.

f) Text Books

Microchip Manufacturing, by S. Wolf, Lattice press
ISBN: 0-961672-8-8

g) Course Outline

- Introduction/Review of symbols, terminology, and notation of Semiconductor Process Technology.
- ITRS/Moore's law
- Overview of process technology, and fabrication steps.
- The PN junction, device physics/carrier concentrations and related equations.
- The MOS transistor and it's 4-terminal operation/related equations. Properties of MOS capacitors, and resistors.
- Design of Wafer Fabrication Process flows
- Wafer Fab equipment understanding
- Process Modeling thru Supreme programs
- Understanding Process Cross sections. SEM/doping profiles
- Relation between process parameters and electrical parameters.
- Cost model/Economics of wafer fabrication
- Safety issues involve in Semiconductor process steps.
- Wafer Fabrication facility design
- Post CMOS devices

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Technician

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Applied Electricity and Electronics Fundamentals (EE-100)

b) Objectives:

This course introduces the students to the exciting world of electricity and electronics through theory and practice. By using several hands-on projects students learn basic to advanced principles behind the working of ubiquitous electrical and electronic circuits.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Electronic Circuit Fundamentals, Floyd, Prentice Hall

g) Course Outline

- Concepts of Work, Power and Energy
- Principles of Electricity
- Concepts of Electric Circuits
- Electric Circuit Components
- Dc Circuits
- Series Circuits
- Parallel Circuits
- Combination Circuits
- Voltage Divider Circuits
- Bridge Circuits
- Calculate Conductor Resistance
- Three-Wire (Edison) Circuits
- Principles of Electromagnetism
- Reading and Interpreting Electrical Drawings
- Electrical Code and Wiring
- AC Fundamentals
- Trigonometry in Electrical Calculations
- Using Vectors in Electrical Calculations
- Principles of Alternating Current
- Single-Phase Ac Circuits
- Principles of Inductance
- Principles of Capacitance
- Effects of Inductive Reactance
- Effects of Capacitive Reactance
- Circuit Protection Devices
- Circuit Protection Devices
- Transformer Fundamentals
- Voltage Regulation
- Lighting Fundamentals
- Incandescent Lighting Circuits
- Fluorescent Lighting Circuits
- Introduction to Electronics
- Transistors, Didoes, Thyristor
- Transistor Circuits
- Introduction to Digital Logic
- Op-Amp Circuits
- Basic Computer Hardware and Software
- Basic Computer Operating Systems and Networks
- Digital Logic Circuits

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Technician

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

National Electrical Code (NEC) Training (EE-110)

b) Objectives:

This course is intended to explain the requirements of the National Electrical Code® and provides basic instruction on the newest editions. It discusses rules to minimize risk of electricity as a source of electric shock and as an ignition source of fire. The course further clarifies and refines student's grasp of grounding.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

NFPA 70 2011 National Electrical Code

g) Course Outline

- Use and Identification of Grounded Conductors Branch Circuits
- Feeders
- Branch-Circuit, Feeder and Service
- Calculations Outside Branch Circuits and Feeders
- Services
- Overcurrent Protection
- Grounding
- Transient Voltage Surge Suppressors
- Wiring Methods
- Conductors for General Wiring
- Cabinets, Cutout Boxes, Meter Socket Enclosures Outlet, Device, Pull, and Junction Boxes; Conduit Bodies; Fittings; and Manholes Armored Cable: Type AC
- Nonmetallic-Sheathed Cable: Types NM, NMC and NMS
- Flexible Metal Conduit: Type FMC
- Liquidtight Flexible Metal Conduit: Type LFMC Rigid Nonmetallic Conduit: Type RNC
- Liquidtight Flexible Nonmetallic Conduit: Type LFNC Electrical Nonmetallic Tubing: Type ENT
- Auxiliary Gutters
- Cablebus
- Metal Wireways
- Busways
- Surface Metal Raceways
- Surface Nonmetallic Raceways
- Cable Trays Flexible Cords and Cables
- Fixture Wires
- Switches
- Receptacles, Cord Connectors, and Attachment Caps Switchboards and Panelboards
- Luminaries, Lamp holders, Lamps
- Appliances
- Fixed Electric Space-Heating Equipment
- Motors, Motor Circuits, and Controllers, including Disconnecting Means for Motors
- Air Conditioning and Refrigeration Equipment Transformers and Transformer Vaults
- Equipment over 600 Volts, Nominal Special Occupancies
- Special Equipment
- Special Conditions
- Communication Systems

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Technician

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Digital Logic Design Fundamentals (EE-120)

b) Objectives:

The course provides a modern introduction to logic design and the basic building blocks used in digital systems. The course starts with a discussion of combinational logic including logic gates, minimization techniques, arithmetic circuits and modern logic devices such as field programmable logic gates. The second part deals with sequential circuits: flip-flops, synthesis of sequential circuits, case studies including counters, registers, random access memories. State machines will be discussed next and illustrated through case studies of more complex systems using programmable logic devices. Different representations including truth table, logic gate, timing diagram, switch representation, state diagram, algorithmic state machine (ASM) chart will be discussed.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Logic and Computer Design Fundamentals, by M. Mano and C. Kime, Prentice Hall
ISBN# 0138134006

g) Course Outline

- Principles of Boolean Algebra to manipulate and minimize logic expressions
- Use of K-maps to minimize and optimize two-level logic functions up to 5 variables
- Operation of latches, flip-flops, counters, registers, and register transfers
- Analyze the operation of sequential circuits using built with various flip-flops
- Concepts of data paths, control units and micro-operations and building block of digital systems

h) Education Requirements
AA or higher

i) Course Level
Entry Level, Technician, Engineering

j) Method of Instruction
On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

MATLAB for Engineering and Scientific Applications (EE-130)

b) Objectives:

This course is designed around learning MATLAB and applying it to a variety of engineering and scientific/research problems. The essentials of MATLAB are taught. These lessons are combined with instructions on fundamental simulation techniques and concepts. The objective of this course is to acquaint students with the basic tools as well as some of the techniques needed to use MATLAB software properly for solving many challenging projects.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

This course has no text book. Course workbook will be provided to students by the school.

g) Course Outline

- Brief history of Matlab
- Introduction to matlab desktop and programming environment
- A few basic commands
- Arithmetic operations
- Data structures in MATLAB, entering data into MATLAB
- Generating arrays and matrices
- Array and matrix indexing and operations
- Matrix algebra vs. element-by-element operations
- Linear Algebra and Eigenvalue Problems
- Root Finding
- Curve Fitting to Measured Data
- Logical operations (AND, OR, XOR,…)
- MATLAB commands
- MATLAB built-in functions
- Plotting in Matlab: 2D & 3D plots , colorbar and colormap
- Symbolic Manipulation in MATLAB
- MatLab I/O
- MATLAB sound capabilities
- MATLAB scripts (M-files)
- MATLAB Programming: Loop constructs & Conditional statements (if, elseif, while, break, etc.)
- MATLAB functions
- MATLAB Toolboxes

h) Education Requirements

AA or higher

i) Course Level

Entry Level, Technician, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

IC Layout Design (EE-150)

b) Objectives:

One of the best training courses available in industry, this course introduces the students to the process, tools and methodology of IC Layout Design using the latest Design Automation tools. The course provides the students with the insight into the exciting field of semiconductor technology and electronic devices, and trains them in IC layout techniques for a variety of application in Digital, Analog, and RFIC. This training program prepares students for entry-level positions in the industry.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

This course has no text book. Course workbook will be provided to students by the school.

g) Course Outline

- Basic Electricity
- Basic Electronics
- Materials properties
- Conductors, Insulators, and Semiconductors
- Electronic Devices
- Resistors
- Transistors
- Diodes
- Capacitors
- Inductors
- Semiconductor processing
- Design Process Overview
- Electronic Circuits
- Analog, Digital, Mixed Signals
- Logic Gates
- Standard Cells
- Gate Arrays
- ASIC Design Methodology
- Standard Cell Library Design
- Diffusion Merging
- Combinational and Sequential Logic
- Floor Planning
- Power Grids
- IO Cells
- Latchup theory & prevention
- ESD Devices
- IC Layout Techniques
- Memory Layout Issues
- Bonding pad, Seal-ring, Scribe-line layout techniques.
- Power bus routing, bus slotting, and Clock net routing techniques
- Unix Training
- UNIX vi editor

h) Education Requirements

High school or higher

i) Course Level

Entry Level, Technician, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

IC Layout Verification (EE-160)

b) Objectives:

This is an advanced hands-on course in the layout and verification of integrated circuits. Students study advanced design layout methods and employ specialized CAD tools to layout and verify circuits. This Layout Verification course is designed to show the students the fundamentals and essentials of DRC, LVS for those who have basic layout background.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

This course has no text book. Course workbook will be provided to students by the school.

g) Course Outline

- Design Flow
- Layout verification flow
- Boolean Operations
- Review of Design Rules
- DRC Flow
- DRC Rule File Creation
- Antenna Effects
- Density Check
- Identify DRC Errors
- LVS Rule File Creation
- Identify and Fix LVS Errors
- Various Hands-on Projects

h) Education Requirements

AA or higher

i) Course Level

Entry Level, Technician, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

MEM Design & Technology Fundamentals (EE-170)

b) Objectives:

This is an advanced hands-on course in the layout and verification of integrated circuits. Students study advanced design layout methods and employ specialized CAD tools to layout and verify circuits. This Layout Verification course is designed to show the students the fundamentals and essentials of DRC, LVS for those who have basic layout background.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

MEMS & Microsystems Design and Manufacture", by Tai-Ran Hsu

g) Course Outline

- Introduction to MEMS design
- Introduction to MOS Technology: Basic MOS Circuit, MOS Circuit Design
- MOS fabrication process: NMOS mask layout and L-Edit software
- MOSIS foundry service
- Integrated CMOS/MEMS Devices: A CMOS Thermal Isolated Gas Flow Sensor
- Micro Hot Wire
- CMOS Fabricated Micromechanical Structures
- Introduction to Accelerometer
- Accelerometer design based on MOSIS rules
- Bulk micro-machined accelerometer: static, dynamic, sensor system and fabrication
- MUMPS Foundry Services: Micro motor design
- Electrostatic micro actuator: Comb drive design
- Magnetic actuator
- Thermal actuator
- Piezoelectric actuator
- Shape memory alloy actuator
- Pneumatic actuator
- Term project presentation

h) Education Requirements

AA or higher

i) Course Level

Entry Level, Technician, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

PCB and PWB Technology Fundamentals (EE-180)

b) Objectives:

This course explores fundamentals of PCB and PWB technologies, applications, design, and test. During the course students are introduced to the application of printed circuit board, materials properties, manufacturing techniques, components; surface mount and through hole, and general design & test methodologies, etc.. The course prepares the students for more advanced programs in PCB design.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Clyde F. Coombs Jr., "COOMBS' PRINTED CIRCUITS HANDBOOK", McGraw-Hill Professional

g) Course Outline

- Connectivity
- Types of boards
  - Single sided
  - Double Sided
  - Multilayer PCB
- Surface Mount components
- General Design Considerations
- Mechanical Design Factors
- Board Size and Shapes
- Material Selection
- Electrical Design Factors
- Environmental Factors
- Layout Standards
- Base Materials
- Circuit Components and Hardware
- Fabrication Process
- Image Transfer
- Plating
- Etching
- Bare Board Testing
- Assembly
- Test in Assembly
- Multilayer Materials
- Flexible Circuits

h) Education Requirements
AA or higher

i) Course Level
Entry Level, Technician, Engineering

j) Method of Instruction
On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

PCB Layout Design (EE-185)

b) Objectives:

This course introduces students to the process, tools, and methodology of the PCB layout design. During the course students will develop basic skills in the use of the modern PCB layout design software and techniques. Schematics, printed circuit board layouts, symbols, and wiring diagrams will be produced on CAD workstation; terminology and the manufacturing process of printed circuit boards will be covered. The course prepares the students for the entry-level PCB layout position.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Required: None

g) Course Outline

- Design Process Overview
- Common User Interface
- Invoking PCB Tools
- Design Creation Terminology
- Design Hierarchy
- Opening Down into a Component
- Process for Preparing a Schematic
- Placing Symbols on the Schematic Sheet
- Adding Wires
- Adding Properties
- Extracting Information from the Design
- Checking and Saving the Design
- Basic Geometry Types
- Display Layers
- Library Management
- Default Directory Hierarchy
- Saving Geometries
- Creating New Geometries
- Attributes
- Adding Geometry Pins
- Checking Geometries
- Introduction to Design Rules
- Mapping Files
- Creating a Part Number
- Checking Part Number Data
- Back Annotation
- Display Controls
- Component Labels
- Setting Display Attributes
- Component Height
- Placement Regions
- Interactive Placement - by Reference, by Connectivity, from Schematic
- Moving and Rotating Components
- Protecting and Fixing Components
- Mapping Components
- Using Board Station RE Placement
- Design Rules
- Physical Layers
- Rules for Pins and Vias
- Understanding Blind Pins and Blind/Buried Vias
- Routing Design Rules by Net and Layer
- NET_TYPE Property
- Interactive Routing
- Protecting Routing
- Area Fills
- Area Fill Connectivity
- Creating an Area Fill
- Changing Reference Designators
- The Artwork Order
- The Aperture Table
- Creating Artwork Data
- Opening Artwork Data
- Simulating Artwork Data
- The Drill Table
- Drill Data file
- Assigning Drill Symbols to Drill Sizes
- Simulating Drilling
- Drafting and Reports
- Creating a Fabrication Drawing
- Creating an Assembly Drawing
- Basic Drafting
- Adding Dimensions
- Dimensioning Styles
- Manufacturing Reports

h) Education Requirements
AA or higher

i) Course Level
Entry Level, Technician, Engineering

j) Method of Instruction
On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Advanced PCB Layout Design (EE-187)

b) Objectives:

This course introduces students to the advanced topics in PCB layout design. The course will allow students to become familiar with signal integrity analysis at the board level. It addresses transmission lines and their effects on digital circuitry and printed circuit boards. The course will present detailed examples from real-world designs to demonstrate the necessity of understanding signal integrity issues and applying sound signal integrity principles to PCB Design. The course is developed around advanced design methodology and prepares the students for the entry-level PCB layout position.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Required: None

g) Course Outline

- Transmission lines and their effect on digital circuitry
- Printed circuit boards: drivers, receivers, Zo, Zdiff, stack up
- Quality board designs
- Termination, topology, timing, parasitics, etc
- Crosstalk: understanding and preventing
- Differential pair: termination, routing, timing, EMI
- Clock distribution, high speed busses, ground bounce
- Reference planes: ground, power, return currents, splits
- High speed layout: vias, connectors, capacitors, losses
- Testing issues: equipment, probes, test points
- Models: SPICE, IBIS, drivers, receivers, simulators and accuracy
- PCB simulations that detect signal integrity problems before fabrication

h) Education Requirements

AA or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

IC Packaging Fundamentals (EE-190)

b) Objectives:

This course provides an overview and a comparison of electronic systems packaging technologies. It includes design; manufacturing; test; IC package assembly; thermal and reliability issues. The course is developed around advanced design methodology and prepares the students for the entry-level position.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Required: Fundamentals of Microsystems Packaging, by Rao Tummala, Publisher: McGraw-Hill Professional

g) Course Outline

I Overview of IC Packaging Technology
1. What is IC Packaging?
2. IC Packaging Roadmap
3. Technology Driving Forces
4. Rent's Rule
5. Hermatic vs. Nonhermatic Packages
6. Multidiscipline Issues

II Manufacturing Considerations
1. Die Attach Technology
2. Die Interconnect Technology
3. Die Coating
4. Plastic Package Manufacturing Process
5. Ceramic Package Manufacturing Process
6. Metal Can Package Manufacturing Process
7. Multichip Module
8. Environmental Control: ESD & Cleanroom Classification
9. Quality and Reliability Issues

III Design Considerations
1. Electrical
1.1 Reflection Noise
1.2 Crosstalk Noise
1.3 Switching Noise
1.4 Signal Attenuation and Dispersion
2. Thermal
2.1 Thermal Resistance
2.2 Heat Flow Mechanisms
3. Mechanical
3.1 Coefficient of Thermal Expansion (CTE)
3.2 Thermal Stress and Strain Distribution Management

IV Electrical Test
1. Electrical PerformanceTesting
2. Electrical Test Methods
3. Electrical Analysis

V Emerging Technologies
1. Ball Grid Array, Chip-scale package (CSP)
2. Flip Chip, Direct Chip Attach (DCA), Wafer Scale package (WSP)
3. 3D Packaging
4. Known Good Die

h) Education Requirements
AA or higher

i) Course Level
Entry Level, Technician, Engineering

j) Method of Instruction
On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

IC Packaging Design Essentials (EE-192)

b) Objectives:

This course covers the design of packaging for integrated circuits. A description of the various IC packaging options is presented to allow the student to understand the trade-offs between different package types such as perimeter 10 packages versus area array packages. Wire bond and flipchip IC attachment methods are analyzed for physical characteristics such as wire bond pull strength and thermal expansion. Electrical effects of the IC package are analyzed through the use of lattice diagrams and impedance calculations and a description of the manufacturing of the three types of MCMs (MCM-D, MCM-L, and MCM-C) is explored.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Required: Fundamentals of Microsystems Packaging, by Rao Tummala, Publisher: McGraw-Hill Professional

g) Course Outline

1. Introduction and Overview
1.1. Introduction to IC Packaging
1.2. Hierarchy of packaging
1.3. Importance of packaging and functions of the package
1.4. The multiple disciplines required for packaging
1.5. Introduction of package types
1.5.1. PGA
1.5.2. BGA
1.5.3. QFP
1.6. Introduction to advanced packaging technologies
1.6.1. Chip scale packaging
1.6.2. 3D high density packaging
1.6.3. PoP
1.6.4. System in package
1.7. Calculating packaging efficiency
1.8. Estimating 10 requirements using Rent's Rule
2. First Level Interconnect
2.1. Tradition packaging technologies
2.1.1. Wirebond
2.1.1.1.Wedge bonding
2.1.1.2.Ball stitch bonding
2.1.2. Flip Chip
2.1.2.1.Flip chip advantages over wirebond
2.1.2.2.Assembly of flip chip technology
2.1.2.3.Die bump functions
2.2. Wirebond pull strength
2.3. Expansion differentials. 3. Package Characteristics
3.1. Electrical characteristics
3.1.1. Define formulas for calculating impedance on a transmission line
3.1.1.1.Stripline
3.1.1.2.Microstrip
3.1.1.3.Buried stripline
3.1.2. Define formulas for calculating propagation delays.
3.1.3. Use lattice diagrams to analyze reflections.
3.2. Thermal Characteristics
3.2.1. Thermal transport modes
3.2.1.1.Conduction
3.2.1.2.Convection
3.2.1.3.Radiation
3.2.1.4.Newton's Law of Cooling 4. Packaging Design Flow
4.1. A Package Design flow
4.1.1. Modeling the package
4.1.2. Modeling the ICs
4.1.3. Wirebonding
4.1.4. Dynamic manufacturing constraints
4.1.5. Package interconnect and routing
4.1.6. Creating manufacturing data
5. Substrate Assembly
5.1. MCM types
5.1.1. Thin film (MCM-D)
5.1.2. Thick film (MCM-C)
5.1.3. Organic (MCM-L)
5.2. Manufacturing challenges
5.2.1. Etch factor
5.2.2. Planarization
5.3. Assembly techniques
6. Package Reliability and Failure Analysis
6.1. Overstress failures and wearout failures
6.2. Electrical failure mechanisms
6.3. Thermomechanical failure mechanisms
6.4. Chemically induced failure mechanisms
6.5. Multi-chip module yields

h) Education Requirements
AA or higher

i) Course Level
Entry Level, Technician, Engineering

j) Method of Instruction
On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Design Signal Processing Principles and Applications (EE-200)

b) Objectives:

With signal processing becoming ubiquitous in today's computer literate world, a large number of application areas are growing in importance, both in industry and in the research community, such as signal processing for distributed sensor networks, speech, image and video processing, medical image processing, wavelets and multiresolution signal processing, genomic and biomedical signal processing, financial data signal processing, etc. This course will cover some of the theoretical, algorithmic and practical foundations needed to address this litany of problems and applications in signal processing.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Digital Signal Processing: Principles, Algorithms, and Applications, Prentice-Hall
By J. G. Proakis and D. G. Manolakis
Ref: Statistical Digital Signal Processing and Modeling, Wiley, by Monson H. Hayes, (ISBN 0471594318)

g) Course Outline

- Signals, Systems, and Signal Processing
- Discrete-Time Signals and Systems
- The Z-transform and its Applications to the Analysis of LTI Systems
- Frequency Analysis of Signals and Systems
- The Discrete Fourier Transform: Its Properties and Applications
- Efficient Computation of the DFT: Fast Fourier Transforms (FFTs)
- Implementation of Discrete-Time Systems
- Design of Digital Filters: FIR/IIR

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Digital Signal Processing with MATLAB (EE-205)

b) Objectives:

This hands-on course explores the use of MATLAB for Design and Signal Processing. The course introduces various concepts of modern Digital Signal Processing, beginning with basic concepts in discrete time systems, filter design and implementation all the way to advanced concepts of multi-rate systems. In parallel, MATLAB is presented as a tool to verify the theory and SIMULINK to address design issues. Each session consists of a balanced mix of theory and practice.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Digital Signal Processing Using Matlab, Edited by André Quinquis

g) Course Outline

- Introduction.
- Discrete-time signals.
- Discrete-time random signals.
- Statistical tests and high order moments.
- Discrete Fourier transform of discrete signals.
- Linear and invariant disctrete-time systems.
- Infinite impulse response filters.
- Finite impulse response filters.
- Detection and estimation.
- Power spectral density estimation.
- Time-frequency analysis.
- Parametrical time-frequency methods.
- Supervised statistical classification.
- Data compression.

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Embedded System Design Fundamentals (EE-207)

b) Objectives:

This course explores methodologies for systematic design of embedded systems including system specification, architecture modeling, component partitioning, estimation metrics, hardware software co-design. Embedded computing platforms and programming. The course further explains how to put all components of the system such as ASIC, CPU, and glue logic together.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Embedded System Design: A Unified Hardware/Software Introduction, By Frank Vahid and Tony Givargis, John Wiley & Sons; ISBN: 0471386782

g) Course Outline

- Introduction. Design methodology and representation. Current CAD design. System-level design.
- Modeling. FSM models. Event Nets. Data Flow and Control Flow models. Flow Chart-based models. UML. Spec Charts. Uniprocessor and Multiprocessor systems. Application-Specific Architectures. Networks.
- ASIC. Specification and representation of embedded systems. HDL. Behavioral and Structural Hierarchy. Data-driven and Control-driven concurrency. Communication and synchronization. Timing. Logic synthesis algorithms.
- CPU. Embedded computing. ARM-based systems. Computing platform. Program design and analysis.
- Estimation and Verification. Estimation techniques at the system level. Simulation of system level design. Prototyping.
- Applications. Digital Camera, Wireless videophone, and others.

h) Education Requirements

MSEE, MSCS or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Practical Design with DSP (EE-209)

b) Objectives:

Advanced DSP (Digital Signal Processor) chips are increasingly being used to design sophisticated products for communications, instrumentations, etc. This hands-on course introduces the students to DSP system design and implementations using programmable signal processors. Several hand-on laboratory exercises, employing a widely used digital signal processor family, are used in conjunction with the lectures to present the design and implementation aspects.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, 6:00pm-9:00pm.

f) Text Books

Required: NA

g) Course Outline

- Signals and signal characteristics
- Discrete-time signals and systems
- Linear Systems: properties and characteristics, examples
- ADC and DAC: Sampling Theorem, Anti-alias Filter
- DSP Software: Fixed Point, Floating Point, Number Precision, Complex Numbers, Execution Speed
- Tools for DSP System Analysis and Design
- DSP Processors comparison
- TMS320F2812 DSP Architecture
- A DSP Development System TMDSEZD2812 F2812 eZdsp Starter Kit
- Code Composer Studio for DSP System Development
- Convolution: properties and applications
- Discrete Fourier Transform: spectral analysis of signals
- Fast Fourier Transform: some practical applications
- Fast Fourier Transform Implementation
- Frequency Domain Parameters, HP, LP, BP, and BR-Filters
- Finite Impulse Response (FIR) filter Implementation
- Infinite Impulse Response (IIR) filter Implementation
- Moving Average Filters
- Windowed-Sinc Filters
- Filter Comparison
- Audio Processing: Human Hearing, Hi-Fi Audio
- Hand-on Projects:
  - Architectural Overview of the DSK, Programming Development Environment familiarization
  - Peripheral Register Header Files, Reset and Interrupts, System Initialization
  - Analog-to-Digital Converter
  - FIR Filter
  - IIR Filter
  - FFT and spectrum analysis

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

FPGA Design Fundamentals (EE-190)

b) Objectives:

This course is intended for designers new to FPGAs design or programmable logic. Beginning with the architecture of Xilinx and/or Altera FPGA, the course will first provide the essential knowledge required to implement a design successfully using the software tools. The first part of the course will give students a head start on not just a fast design turn, but an elegant design as well. The second part of the course focuses on how to create more efficient designs to enhance overall performance. Student will learn how to create a faster design, fit the design into a smaller FPGA or a lower speed grade, thereby reducing the system cost and development time.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

This course requires no text book.

g) Course Outline

- Basic FPGA Architecture
- Lab 1: Xilinx Tool Flow
- Reading Reports
- Lab 2: Architecture Wizard and PACE
- Global Timing Constraints
- Lab 3: Global Timing Constraints
- Implementation Options
- Lab 4: Implementation Options
- Synchronous Design Techniques Review of Fundamentals of FPGA Design
- Designing with Virtex-4 FPGA Resources
- CORE Generator Software System
- Lab 5: CORE Generator Software System
- Designing Clock Resources
- Lab 6: Designing Clock Resources
- FPGA Design Techniques
- Synthesis Techniques
- Lab 7: Synthesis Techniques Properties and Applications
- Achieving Timing Closure Timing Groups and OFFSET Constraints Lab 9: Achieving Timing Closure
- Advanced Implementation Options
- Lab 10: Designing for Performance
- Power Estimation (Optional)
- Lab 11: FPGA Editor Demo (Optional)
- ChipScope™ Pro Analyzer (Optional)
- Lab 12: ChipScope Pro Analyzer (Optional)

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Automated Test and Measurement with LabVIEW (EE-140)

b) Objectives:

This course is developed around using National Instrument's LabVIEW software and intends to teach students how to configure a wide variety of measurement, signal generation, RF, power, and switch modules in NI LabVIEW and other software to meet their specific test and measurement tasks.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

This course requires no text book.

g) Course Outline

- Identifying the steps in the software development
- method
- Defining a problem
- Designing an algorithm, flowchart, or state transition
- diagram
- Preparing for implementation, testing, and maintenance of applications
- Designing a user interface (LabVIEW front panel)
- Choosing data types and displaying data as a plot
- Using structures like the While loops and For loops
- Adding software timing to your code
- Making decisions in your code using case
- structures
- Documenting your code
- Plug-in DAQ devices – typical hardware
- characteristics
- Data acquisition in LabVIEW – software
- architectures
- Simulating a DAQ device
- Performing analog input and output
- Counters
- Performing digital input and output
- Single loop architectures – simple VI, general VI, and the state machine design patterns
- · Multiple loop architectures – parallel loop VI, the master/slave, and the producer/consumer design
- patterns
- · Parallelism
- · Adding timing to a design pattern
- VI server architecture
- · Property nodes
- · Control references
- · Invoke nodes

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Digital VLSI IC Design with Verilog (EE-210)

b) Objectives:

This hands-on course presents to the students the design of digital integrated circuits using the Verilog digital design language as described in IEEE Standard 1364-2001. By a balanced mixture of lectures and labs, the students are introduced to language constructs in a progressively more complex project environment. During the course, students will become familiar with the use of the Synopsys Design Compiler to synthesize gate-level netlists from behavioral, RTL, and structural Verilog code. The synthesis constraints most useful for area and speed optimization are emphasized. Almost all work is done in the synthesizable subset of the language; logic simulation is treated as an occasional verification method. Other topics include design partitioning, hierarchy decomposition, safe coding styles, assertion-based verification, and design for test.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Required: M.D. Ciletti, "*Modeling, Synthesis, and Rapid Prototyping with Verilog HDL*" Prentice Hall,1999

Reference: D.E. Thomas and P. Moorby, "*The Verilog Hardware Description Language*" 3rd. Edition, KluwerAcademic Press, 1996.

g) Course Outline

- Modules and hierarchy
- Blocking/nonblocking assignment
- Combinational logic
- Sequential logic
- Behavioral modelling
- RTL modelling
- Gate-level modelling
- Hardware timing and delays
- Verilog parameters
- Basic system tasks
- Timing checks
- Generate statement
- Simulation event scheduling
- Race conditions
- Synthesizer operation
- Synthesizable constructs
- Netlist optimization
- Synthesis contol directives
- Verilog influence on optimization
- Use of SDF files
- Test structures
- Error correction basics
- Hand-on Projects:
    - shift and scan registers
    - counters
    - memory and FIFO models
    - digital phase-locked loop (PLL)
    - serial-parallel (and v-v) converter
    - serializer-deserializer (SerDes)
    - primitive gates
    - switch-level design
    - netlist backannotation

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Timing Verification of Digital VLSI Designs (EE-215)

b) Objectives:

This is a course covering timing verification during the complete netlist-to-tapeout backend flow in a typical suite of EDA tools. Simulation and other functional verification is held to a minimum.
A full-duplex serdes design totaling some 250,000 transistors equivalent, is used for the majority of exercises and illustrations requiring design hierarchy. Using the Synopsys® tools, synthesis constraints on the original verilog source first are explored in detail; then, the resulting netlist is floorplanned, placed-and-routed, and converted to a tape-out mask definition format. Static timing verification is exercised in all tools supporting it, at all stages of the process.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Required: Bhatnagar, H. Advanced ASIC Chip Synthesis Using Synopsys. Design Compiler. Physical Compiler. and Primetime. Norwell, Massachusetts: Kluwer Academic, 2001.

g) Course Outline

- Basic tool flow from synthesis through tape-out. TcL and SDC in the Synopsys tools; TcL Basics; SDC Basics. The Milkyway database. HDL partitioning and optimization. Synthesizer scripts, design rules, and constraints. Clock constraints, delay constraints, and critical paths.
- HDL embedded synthesis scripts. Characterization of submodules. Advanced synthesis and optimization controls. Technology-library modelling. Basics of Liberty syntax and Liberty-ALF similarities. Cell characterization overview. Design netlist and extracted models. QTM models.
- Design interface-logic models (ILM) vs extracted HTV models. Design-block STAMP models. STAMP syntax and extracted STAMP models.
- The JupiterXT floorplanner, design flow, and the Flow Manager. Flat vs hierarchical floorplans, placement plan groups, and pad placement. Cells, flylines, and floorplan reports. Jupiter feasibility analysis, back-annotation, and constraints. SDF coordination.
- Incremental resynthesis. Jupiter ECO's. Astro Introduction. Floor-planning and incremental changes. PrimeTime with a floor-plan; PrimeTime ECO's.
- Fully-placed timing verification. Placement legalization, global routing, and final-placement flow. Clock tree timing and use of the IC Compiler.
- IC Compiler and fully-placed SDF. SPEF features and basic parameters.
- PrimeTime and placement. Detailed routing flow.
- IC Compiler features and constraints. Parasitics, crosstalk, and timing. Pin separation and extraction of HTV timing.
- Effects of routing on timing. PrimeTime fully-routed verification. PrimeTime ECO of final netlist.
- Tape-out conversion; mask-definition formats; automated GDS2 or OASIS generation.

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Design of Digital CMOS Integrated Circuits (EE-300)

b) Objectives:

This course provides a detailed review of the principles, concepts, and design methods used in the design of basic digital circuits using CMOS technology. The course will begin with a brief review of background information (i.e. fabrication technology, CMOS device physics, and related device equations), and then proceed to common digital building blocks and more complex digital circuits. Computer simulations are be used extensively to enhance the learning experience.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

CMOS DIGITAL INTEGRATED CIRCUITS by Kang and Leblebici, ISBN: 0072460539, San Francisco, McGraw-Hill

g) Course Outline

- Basics of MOSFET operation and SPICE modeling
- MOS inverters: static characteristics
- MOS inverters: dynamic operation
- CMOS Layout and Simulation
- Combinational MOS logic circuits
- Sequential MOS logic circuits
- Dynamic MOS logic circuits
- Semiconductor memories

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Design of Analog CMOS Integrated Circuits (EE-310)

b) Objectives:

Modern integrated circuit design is broadly divided into analog and digital design. This course provides a detailed review of the principles, concepts, and design methods used in the design of current state-of-the-art CMOS analog circuits. The course will begin with a brief review of background information (i.e. fabrication technology, CMOS device physics, and related device equations), and then proceed to common analog building blocks and more complex analog circuits. Computer simulations are be used extensively to enhance the learning experience.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

CMOS Analog Circuit Design
by Phillip E. Allen and Douglas R. Holberg
ISBN: 0-19-510720-9

g) Course Outline

- Introduction/Review of symbols, terminology, and circuit notation of analog systems.
- Overview of process technology, and fabrication steps. The PN junction, device physics/carrier concentrations and related equations. The MOS transistor and it's 4-terminal operation/related equations. Properties of MOS capacitors, and resistors.
- Large-Signal FET model. Output characteristics of MOS transistor. Nonideal/parasitic device models/effects within MOS transistor. Small-Signal FET model.
- Analog building blocks: MOS switch, active resistors/loads, voltage dividers, current sinks/sources, cascode current sink, current mirrors, cascode current mirrors, Wilson current mirrors, current/voltage references, and bootstrap references.
- Amplifiers: simple inverters, current-sink inverter, push-pull inverters, differential amplifiers, cascode amplifiers, simple output amplifiers, source-follower amplifiers, push-pull source follower, and high gain amplifiers.
- Comparators: first order models, inverting comparators, differential input comparators, two-stage comparators, comparator hysteresis, and auto-zeroing techniques.
- Operational Amplifiers: non-ideal models, frequency response, compensation, two-stage operational amplifiers, cascode operational amplifiers, differential Cascade stages, cascode output stages, calculation of power supply rejection ratios, folded cascode operational amplifiers, open loop characteristics, common mode rejection ratios, and common mode gain

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Advanced Analog CMOS IC Design (EE-310)

b) Objectives:

Modern integrated circuit design is broadly divided into analog and digital design. This course provides a detailed review of the principles, concepts, and design methods used in the design of current state-of-the-art CMOS analog circuits. The course will begin with a brief review of background information (i.e. fabrication technology, CMOS device physics, and related device equations), and then proceed to common analog building blocks and more complex analog circuits. SPICE simulations will be used extensively to augment the text/lecture material.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

CMOS Analog Circuit Design
by Phillip E. Allen and Douglas R. Holberg
ISBN: 0-19-510720-9

g) Course Outline

- Introduction/Review of symbols, terminology, and circuit notation of analog systems.
- Overview of process technology, and fabrication steps. The PN junction, device physics/carrier concentrations and related equations. The MOS transistor and it's 4-terminal operation/related equations. Properties of MOS capacitors, and resistors.
- Large-Signal FET model. Output characteristics of MOS transistor. Nonideal/parasitic device models/effects within MOS transistor. Small-Signal FET model.
- Analog building blocks: MOS switch, active resistors/loads, voltage dividers, current sinks/sources, cascode current sink, current mirrors, cascode current mirrors, Wilson current mirrors, current/voltage references, and bootstrap references.
- Amplifiers: simple inverters, current-sink inverter, push-pull inverters, differential amplifiers, cascode amplifiers, simple output amplifiers, source-follower amplifiers, push-pull source follower, and high gain amplifiers.
- Comparators: first order models, inverting comparators, differential input comparators, two-stage comparators, comparator hysteresis, and auto-zeroing techniques.
- Operational Amplifiers: non-ideal models, frequency response, compensation, two-stage operational amplifiers, cascode operational amplifiers, differential Cascade stages, cascode output stages, calculation of power supply rejection ratios, folded cascode operational amplifiers, open loop characteristics, common mode rejection ratios, and common mode gain

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Design of Radio Frequency Integrated (RFIC) Circuits (EE-330)

b) Objectives:

This program covers the design techniques, devices, tools and methodologies for design of integrated radio frequency circuits. The course introduces the students to the current wireless transceiver architectures and provides the students with deep insight into the physics, characteristics and design of passive components (inductor, capacitor) and active devices. This course will further trains the students in the IC design for advanced RF applications such as high speed amplifiers, LNA, Mixer, VCO, PA, PLL and synthesizers.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Required: Thomas H. Lee*, The Design of CMOS Radio-Frequency Integrated Circuits,* Cambridge University Press, 1998.
Reference: Behzad Razavi, *RF Microelectronics*, Prentice-Hall 1998

g) Course Outline

- Introduction to Radio Frequency Integrated Circuits and wireless transceiver architectures
- Physical quantities and their logarithmic representations: dB, dBm, dBV, dBA
- Devices: diode, BJT, MOS
- Modeling of passive/active integrated devices
- Signal sources: ideal vs. real.
- Limitations of analog circuits:
    - Noise & distortion.
    - Nonlinear distortion
- Measures of distortion:
    - Compression
    - Desensitization
    - Inter-modulation
- Nonlinearity and negative feedback.
- Overview of monolithic bipolar and CMOS:
    - LNA's
    - Mixers
    - Filters
    - Broadband amplifiers
    - RF power amplifiers
    - VCO's, and frequency synthesizers
- Analysis of noise and non-linearity in RFIC's

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Advanced RFIC Design (EE-340)

b) Objectives:

This program covers the design techniques, devices, tools and methodologies for design of integrated radio frequency circuits. The course introduces the students to the current wireless transceiver architectures and provides the students with deep insight into the physics, characteristics and design of passive components (inductor, capacitor) and active devices. This course will further trains the students in the IC design for advanced RF applications such as high speed amplifiers, LNA, Mixer, VCO, PA, PLL and synthesizers.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Required: Thomas H. Lee*, The Design of CMOS Radio-Frequency Integrated Circuits,* Cambridge University Press, 1998.
Reference: Behzad Razavi, *RF Microelectronics*, Prentice-Hall 1998

g) Course Outline

- Introduction to Radio Frequency Integrated Circuits and wireless transceiver architectures
- Physical quantities and their logarithmic representations: dB, dBm, dBV, dBA
- Devices: diode, BJT, MOS
- Modeling of passive/active integrated devices
- Signal sources: ideal vs. real.
- Limitations of analog circuits:
- Noise & distortion.
- Nonlinear distortion
- Measures of distortion:
- Compression
- Desensitization
- Inter-modulation
- Nonlinearity and negative feedback.
- Overview of monolithic bipolar and CMOS:
- LNA's
- Mixers
- Filters
- Broadband amplifiers
- RF power amplifiers
- VCO's, and frequency synthesizers
- Analysis of noise and non-linearity in RFIC's

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Design of Low Power Digital Integrated Circuits (EE-350)

b) Objectives:

This course introduces students to IC design for low power and energy consumption. Some of the topics covered are: Low power architectures, logic styles, and circuit design. Variable supply and threshold voltages. Leakage management. Power estimation. Energy sources, power electronics, and energy recovery. Course will also include applications in portable electronics and sensors, and Thermodynamic limits.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Required: Low Power Design Essentials (Integrated Circuits and Systems) by Jan Rabaey
Reference: Roy, K. and Prasad, S., Low Power CMOS VLSI: Circuit Design
Chandrakasan, A. and Broderson, R., eds., Low-Power CMOS Design

g) Course Outline

- Overview of Low Power Design
  - CMOS Power Dissipation
  - Power and Performance Tradeoffs
  - Trends in IC Power Consumption
- Low Power Architectures
  - Clock Gating and Clock Management
  - Pipelining to Reduce Supply Voltage
  - Parallelization to Reduce Supply Voltage
- Low Power Circuit Design
  - Logic Power Estimation
  - Power Minimization in Static CMOS
  - Power Minimization in Dynamic CMOS
  - Multiple-Threshold CMOS
  - Variable Supply and Threshold Voltages
  - Managing Leakage
  - Subthreshold Circuit Design
  - Silicon-on-Insulator (SOI) Technologies
  - Energy Recovery
  - Interconnect Power Estimation and Management
- Energy Sources and Power Electronics
  - Batteries and Fuel Cells
  - Energy Scavenging
  - DC/DC Converters: Fundamentals
  - DC/DC Converters: Optimization
- Other Topics in Low Power Design
  - Low Power Synthesis
  - Applications: Computing, Communication, and Multimedia
  - Applications: Sensors and Sensor Networks
  - Fundamental Limits and Thermodynamics of Computation

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Low Power VLSI Design (EE-370)

b) Objectives:

The course explores in adequate detail various practical design methodologies for improving the power performance of SoC products. Among the design concepts covered in this course are: Clock Gating, Power Gating, Multivoltage Designs, Multi-threshould techniques, etc. In addition to lecture notes in PowerPoint, course includes several detailed labs where students can gain a closer understanding of the concepts and become familiar with the underlying design methodologies and flows.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Required: Low power VLSI design manual co-authored by ARM, Renesas and Synopsys

g) Course Outline

- Power vs. Energy
- Dynamic Power
- Conflict between Dynamic and Static Power
- Static Power
- Clock Gating
- Gate Level Power Optimization
- Multi VDD
- Multi-Threshold Logic
- Challenges in Multi-Voltage Designs
- Voltage Scaling Interfaces – Level Shifters
- Automation and Level Shifters
- Level Shifter Recommendations and Pitfalls
- Timing Issues in Multi-Voltage Designs
- Power Planning for Multi-Voltage Design
- System Design Issues with Multi-Voltage Designs
- Level Shifters – High to Low Voltage Translation
- Level Shifters – Low-to-High Voltage
- Level Shifter Placement
- Dynamic and Leakage power profiles
- Principles of Power Gating Design
- Power Switching – Fine Grain vs. Coarse Grain
- The Challenges of Power Gating
- Impact of Power Gating on Classes of Sub-systems
- Switching Fabric Design
- Signal Isolation
- State Retention and Restoration Methods
- Power Gating Control
- Power Gating Design Verification
- Design For Test considerations
- Hierarchy and Power Gating
- Power State Tables and Always On Regions
- Power Networks and Their Control
- On-chip Power Gating
- External Power Rail Switching
- Fundamental Limits

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

INTERNET OF THINGS (IOT) FUNDAMENTALS (EE-175)

b) Objectives:

This course explores the core technologies behind Internet of Things. The course covers the fundamental technologies enabling IoT such as infrastructure, communication, sensor technologies, networking technologies, data/storage/analytics and security aspects of IoT in building the next-generation computing realm, which makes a world fully connected.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

The Silent Intelligence: The Internet of Things,
by Daniel Kellmereit and Daniel Obodovski

g) Course Outline

Introduction to IoT
• What is IoT?
• Effects of IoT
• Skill set for IoT
• Challenges and barriers to IoT
• Functional Requirements of IoT
Overview of IoT
• Communication aspects involved in IoT system
Wired connectivity and technologies
Wireless connectivity and technologies
• Power and Energy Management & Optimization
• Network Topologies for IoT
• IoT Protocols
• IoT – Technologies & Software
Components & Elements of IoT
• Components of IoT
• Elements of IoT
Visualization
Security
Architecture of IoT system
• Internet of Things—Architecture – IoT-A
• The IoT-A Reference Model
• Cloud Computing
—-o Cloud Computing in Internet of Things
—-o Internet of Things with Cloud Architecture
—-o IoT-related Cloud Security Issues
—-o IoT-related Cloud Computing Privacy Issues
—-o Building a Private Cloud to enable IoT
• Business Analytics
—-o Business Analytics in IoT Architecture
—-o IoT and Data Mining
—-o Data Warehouse in IoT
—-o Data Visualization and Tools in
—-o Understanding Big Data
—-o Hadoop and MapReduce
—-o Apache HBase
Databases for IoT
• Big Data turning into “HUGE DATA”
• SQL Databases
• NoSQL Databases
• Cloud Databases
Mobile integration to enable IoT
• Mobile Middleware
• Omni-Channel Retailing
• Mobile Loyalty
• Mobile Point of Sale
• Mobile Inventory
• Real World Mobile Integration Examples
Security Aspects of IoT
• IoT Security Aspects
• IoT features leading to security issues
• Security Issues in IoT based on RFID
• Design Considerations for IoT Technologies
Privacy Aspects of IoT
• Privacy Analysis

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

INTERNET OF THINGS (IOT) DESIGN & APPLICATION (EE-185)

b) Objectives:

This course is a follow up to the "IoT Fundamentals" course, and explores several examples of IoT applications. It is intended to be a hands-on training program where students will design and assemble IoT devices for various applications.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Internet of Things (A Hands-on-Approach) Paperback
by Vijay Madisetti (Author), Arshdeep Bahga

g) Course Outline

- Configure at least one integrated development environment (IDE) for developing software.
- Make use of git, adb and fastboot to flash multiple OS and repair bricked boards.
- Install Android 5.1 (Lollipop) and Linux based on Ubuntu.
- Create, compile and run a Hello World program.
- Describe the DragonBoard™ 410c peripherals, I/O expansion capabilities, Compute (CPU and Graphics) capabilities, and Connectivity capabilities.
- Estimate sampling frequency and bit-width required for different sensors.
- Program GPIOs (general purpose input/output pins) to enable communication between the DragonBoard 410c and common sensors.
- Write data acquisition code for sensors such as passive and active infrared (IR) sensors, microphones, cameras, GPS, accelerometers, ultrasonic sensors, etc.
- Write applications that process sensor data and take specific actions, such as stepper motors, LED matrices for digital signage and gaming, etc.
- Implement session initiation, management and termination on your DragonBoard™ 410c using SIP.
- Compare and contrast narrowband and wideband codecs and experience the voice quality differences between them.
- Implement and demonstrate VoIP calls using the DragonBoard 410c.
- Explain the tradeoffs between media quality and bandwidth for content delivery.
- Extract and display metadata from media files.
- Implement and demonstrate a simple media player application using DragonBoard™ 410c.
- Design systems using mobile platforms.
- Develop systems that interface multiple sensors and actuators to the DragonBoard™ 410c system and develop the necessary software to create a fully functional system.

h) Education Requirements

BSEE or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

SCRUM MASTER AND JIRA TRAINING (EM-115)

b) Objectives:

Scrum is an Agile framework for completing complex projects. Scrum originally was formalized for software development projects, but it works well for any complex, innovative scope of work. This course covers the principles and theory underpinning the mechanics, rules and roles of the Scrum framework. Students learn through instruction and team-based exercises, and are challenged to think in terms of the Scrum principles to better understand what to do when returning to the workplace.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

The Scrum Guide
by Ken Schwaber and Jeff Sutherland

g) Course Outline

Scrum
Why move to Scrum/Agile? – 3 Case studies.
Empirical Process Control Theory: Transparency, Inspection, Adaptation
Product Owner tasks and responsibilities
Development Team tasks and responsibilities
Scrum Master tasks and responsibilities
Product Backlog maintenance
Sprint Backlog maintenance
Sprint Increment
The Sprint event
Time Boxing
Definition of Done
Sprint Planning event.
Product Backlog grooming
Sprint Backlog creation
Empirical estimation
The Daily Scrum
Tracking progress with a Scrum Board
The Sprint Review
Technical Debt
The four factors of Software Development
The Sprint Retrospective
Taking time during a Sprint to prepare for the next Sprint
Why Scrum works
Transforming the organization
Common obstacles to successful transformation
JIRA
Create a JIRA project
Create and administer JIRA users and security settings
Create a JIRA issue and progress it through the workflow
Monitor the issue status as it flows through the workflow using search
Describe how issues are categorized in JIRA
Save a search to simplify status requests
Modify existing issues, changing priority and assignees
Update multiple issues in one operation to align with changing business requirements
Use versions to coordinate a product release
Experiment with an Agile board to managing multiple issues effectively
Create and use JIRA burndown charts
Link a JIRA issue to a Confluence page
Create a customized JIRA issue screen
Create a customized JIRA workflow
Communicate progress of project tasks using the JIRA dashboard
Create a customized JIRA dashboard.

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 60 consisting of 24 hours of lecture and 36 hours of team projects and Lab

a) Course Title:

SCRUM MASTER BOOT CAMP (EM-110)

b) Objectives:

Scrum is an Agile framework for completing complex projects. Scrum originally was formalized for software development projects, but it works well for any complex, innovative scope of work. This course covers the principles and theory underpinning the mechanics, rules and roles of the Scrum framework. Students learn through instruction and team-based exercises, and are challenged to think in terms of the Scrum principles to better understand what to do when returning to the workplace.

d) Length of program:

The course duration is 2 days.

e) Class Sessions

This is a 2-day training program

f) Text Books

The Scrum Guide
by Ken Schwaber and Jeff Sutherland

g) Course Outline

Scrum
Why move to Scrum/Agile? – 3 Case studies.
Empirical Process Control Theory: Transparency, Inspection, Adaptation
Product Owner tasks and responsibilities
Development Team tasks and responsibilities
Scrum Master tasks and responsibilities
Product Backlog maintenance
Sprint Backlog maintenance
Sprint Increment
The Sprint event
Time Boxing
Definition of Done
Sprint Planning event.
Product Backlog grooming
Sprint Backlog creation
Empirical estimation
The Daily Scrum
Tracking progress with a Scrum Board
The Sprint Review
Technical Debt
The four factors of Software Development
The Sprint Retrospective
Taking time during a Sprint to prepare for the next Sprint
Why Scrum works
Transforming the organization
Common obstacles to successful transformation

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 14 hours consisting of lecture and lab

a) Course Title:

PROJECT MANAGEMENT ESSENTIALS (EM-100)

b) Objectives:

Project Management Essentials is an instructor led training in a formal classroom environment. It is designed to provide personnel with a broad understanding of the project management principles, concepts, tools and techniques applied across the organization, along with the global standards from which they are derived.

d) Length of program:

The course duration is 6 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

A Guide to the Project Management Body of Knowledge: PMBOK(R) Guide
by Project Management Institute

g) Course Outline

Foundations
Formal vs. informal project management
Project management life cycle
Initiating
Role of the project manager
Project charter
Stakeholder identification and assessment
Progressive elaboration
Planning
Planning around project constraints
SMART objectives
Converting objectives into requirements
Decomposition of requirements into a work breakdown structure
Developing a work breakdown structure dictionary
Principles of estimating time and cost
Analyzing work and estimating duration of work packages
Determining sequence of work packages
Network diagramming and critical path analysis
Budgeting resources and cost control
Ensuring that all management responsibility areas are included in the project plan
Analyzing risks for probability and impact
Mitigating and planning risk contingencies
Preparing baselines for scope, time, and cost
Obtaining stakeholder sign-off
Executing, Monitoring, and Controlling
Team-building principles and priorities
Status and performance reporting
Management by exception
Keeping stakeholders informed and involved
Steering performance back to the baseline
Integrated change controls
Closing
Transitioning the product or service
Capturing lessons learned for the organization
Final report to stakeholders
Exercises
Formal vs. Informal Project Management
Analyze Stakeholders
Convert Vague Objectives into SMART Objectives
Create a Work Breakdown Structure
Estimate Effort and Duration for Work Packages
Perform Network Diagramming and Determine Critical Path
Estimate Resource Costs for Work Packages
Analyze and Plan for Risk
Manage Project Change
Review Lessons Learned

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 60 consisting of 24 hours of lecture and 36 hours of team projects and Lab

a) Course Title:

COMPUTER NETWORKING ESSENTIALS (CS-110)

b) Objectives:

Networking Fundamentals teaches the basic concepts and terminology of networking and is designed to prepare students for the CompTIA Network+ Certification Exam. The text covers media types and standards and how data is encoded and transmitted. Students are also introduced to the terminology and basic concepts of each network operating system. The Open Systems Interconnection (OSI) model is introduced as well. A complete chapter is dedicated to TCP/IP and another to sub-netting.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Computer Networking: A Top-Down Approach, 6th edition, by James Kurose and Keith Ross (ISBN-13: 978-0132856201)

g) Course Outline

- Protocol layers and service models. OSI and Internet protocols.
- What is the Internet. Concepts of delay, security, and Quality of Service (QoS).
- Application layer protocols and client-server model.
- Sockets programming in C (client-server and web server programs).
- Reliable data transfer. Stop-and-Go evaluation. TCP and UCP semantics and syntax.
- TCP RTT estimation. Principles of congestion control.
- Principles of routing: link-state and distance vector. IP semantics and syntax.
- Link layer. Error detection. Multiple access protocols. Midterm Exam.
- IEEE 802.3 Ethernet.
- Switching and bridging. Media. Signal strength. Data encoding.
- Wireless and mobile networks.
- Security. Overview of threats, cryptography, authentication, and firewalls.
- Network management including SNMP. Network troubleshooting.
- Hot topics. Sensor networks and Sofware Defined Networks.
- Overflow and course wrap-up
- Final exam

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Cybersecurity Foundations (CS-200)

b) Objectives:

The Cybersecurity Fundamentals Online Course will provide learners with principles of data and technology that frame and define cybersecurity. Learners will gain insight into the importance of cybersecurity and the integral role of cybersecurity professionals. The interactive, self-guided format will provide a dynamic learning experience where users can explore foundational cybersecurity principles, security architecture, risk management, attacks, incidents, and emerging IT and IS technologies.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Dieter Gollmann , Computer Security , 2010
Ross Anderson , Security Engineering , 2008

g) Course Outline

- Critical Business Security
- Worldwide Internet Growth
- Security Fundamentals
- Security Goals
- Terminology Threats and Exposures
- Exploits and Exposures
- Hackers and Crackers
- Attack Methods
- Social Engineering
- Common Attack Vectors
- Traffic Analysis
- Responding to Threats and Attacks
- Documents and Procedures to Manage Risk
- Vulnerability Scanners
- Penetration Testing
- The OSSTMM
- NIST
- Risks of Penetration Testing
- The Structure of the Internet and TCP/IP
- CNCI
- Initiatives
- Legal Compliance Standards
- Acts
- Federal Agency Compliance
- Commercial Regulatory Compliance
- Internet Leadership IANA
- Regional Internet Registry
- Protocols and RFCs
- TCP/IP Model
- Network Access Layer
- Internet Layer
- Host-to-Host Layer
- Process Layer
- Domain Name Service
- Vulnerability Assessment and Tools
- Vulnerabilities and Exploits
- Vulnerability Assessment Tools
- Application-Level Scanners
- System-Level Scanners
- System-Level Testing Tools

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Cybersecurity Implementation (CS-210)

b) Objectives:

The Cybersecurity Implementation Course is a follow up to the "Cybersecurity Foundations" and will provide the students with methods to combat the sybersecurity threats. Students continue to gain insight into the importance of cybersecurity and the integral role of cybersecurity professionals.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Dieter Gollmann , Computer Security , 2010
Ross Anderson , Security Engineering , 2008

g) Course Outline

- Models
- Policies
- Lifecycle
- Distribution
- 13. Firewalls and Edge Devices
- General Security Integration
- Services
- Needs for Services
- Security Zones
- Filtering
- Screened Subnets
- Trusted Zones
- Devices
- Routers
- Firewalls
- DMZ Hosts
- Other Security Considerations
- Business-to-Business Communications
- Exceptions to Policy
- Special Services and Protocols
- Configuration Management
- Software Development Security
- Certification and Accreditation
- Common Criteria
- Intrusion Detection and Prevention
- Defense in Depth
- Network Device Logging
- Host Monitoring and Logging
- Events Correlation
- Placement of IDS Monitors and Sensors
- Monitoring
- Host-Based and Network-Based Differences
- Policy Management
- Behavioral Signatures
- IDS and IPS Weaknesses
- Encryption
- Incorrect Configuration
- Forensic Analysis
- Incident Handling
- Security Incident Response
- Time and Reaction Sensitivity

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

3D Microelectronic System Integration (EE-145)

b) Objectives:

This course will detail the 3D IC integration technologies and applications. The course covers both the fundamental and advanced technologies in use today to produce both stacked chip packages as well as stackable packages for implementation of highly integrated mobile electronic products. These include the challenges of die thinning, thin die attach, multi-level wire bonding, mixed technology die attachment and bonding, flip chip and TAB. Substrate selection for various 3D packaging techniques including silicon tiles, flex circuit origami and specialty interposers concludes the chip-stacking section of the course.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

3D Integration for VLSI Systems 0th Edition
by Chuan Seng Tan (Editor), Kuan-Neng Chen (Editor), Steven J. Koester

g) Course Outline

- 3D Package Trends
- 3D Package Applications
- Drivers for 3D Packaging
- Stacked Packages
- Package on Package
- Origami
- Edge Stacked Modules
- Die Stacking
- Wire Bond
- Mixed Technology
- Edge Redistribution
- Through Silicon Vias
- 3D Integration (SiP)
- Issues in 3D Integration
- Intellectual Property Landscape for 3D Packaging

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Revit Architecture Commercial and MEP (CAD-185)

This course introduces Design Integration Using Autodesk Revit. The course is designed to provide the student with a well-rounded knowledge of Autodesk Revit tools and techniques. All three flavors of the Revit platform are introduced. This approach gives the reader a broad overview of the Building Information Modeling (BIM) process. The topics cover the design integration of most of the building disciplines: Architectural, Interior Design, Structural, Mechanical, Plumbing and Electrical.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Design Integration Using Autodesk Revit 2015: Architecture, Structure and MEP Perfect by Daniel John Stine (Author)

g) Course Outline

Section 1: Introduction to BIM and Autodesk Revit
- 1.1 BIM and Autodesk Revit
- 1.2 Overview of the Interface
- 1.3 Starting Projects
- 1.4 Viewing Commands

Section 2: Basic Drawing and Modify Tools
- 2.1 Using General Drawing Tools
- 2.2 Inserting Components
- 2.3 Selecting and Editing Elements
- 2.4 Working with Basic Modify Tools

Section 3: Basic Systems Tools
- 3.1 Connecting Components
- 3.2 Working with Additional Modify Tools
- 3.3 Creating Systems – Overview

Section 4: Starting Systems Projects
- 4.1 Linking in Revit Models
- 4.2 Setting Up Levels
- 4.3 Copying and Monitoring Elements
- 4.4 Batch Copying Fixtures
- 4.5 Coordinating Linked Models

Section 5: Working with Views
- 5.1 Setting the View Display
- 5.2 Duplicating Views
- 5.3 Adding Callout Views
- 5.4 Creating Elevations and Sections

Section 6: Spaces and Zones
- 6.1 Preparing a Model for Spaces
- 6.2 Adding Spaces
- 6.3 Working with Spaces
- 6.4 Creating Zones
- 6.5 Creating Color Schemes

Section 7: Energy Analysis
- 7.1 Preparing a Project for Energy Analysis
- 7.2 Analyzing the Heating and Cooling Loads
- 7.3 Exporting for Secondary Analysis

Section 8: HVAC Networks
- 8.1 Adding Mechanical Equipment and Air Terminals
- 8.2 Adding Ducts and Pipes
- 8.3 Modifying Ducts and Pipes

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

SketchUp Essentials (CAD-150)

The goal for this class is to provide you with the building blocks to create digital 3D models for the purpose of creating and communicating real world designs. By the end of this course you should feel comfortable making a model from hand-drawn or CAD generated plans. You will learn all of the fundamentals of this program, as well as numerous short cuts and "tricks of the Trade" to ensure that you are as fast and as efficient as you desire.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

The SketchUp Workflow for Architecture: Modeling Buildings, Visualizing Design, and Creating Construction Documents with SketchUp Pro and Layout, 1st Edition
By Michael Brightman (Author)

g) Course Outline

- Introductions and Setup
- • About the instructor/ Introductions
- • What we're going to do: Syllabus
- Review
- • Sample project images
- • About SketchUp: History, Capabilities
- and Uses
- • The Difference between 3D and BIM
- (Building Information Modeling)
- • Interior Space vs. Exterior Space
- Program Setup
- • Opening SketchUp: The Initial Setup
- "out of the box"
- • Using Single and Multiple Screens
- • Preparing the interface and meeting
- "Sophia"
- □ Toolbars and Menus
- □ Saving your setup
- □ Saving space for laptop use
- □ Program Settings
- □ Model Info and Preferences
- • Menu Options, Icon review
- • 3D Space: Axes, Views
- • Orbiting, Zooming and Panning
- Basic Geometry/ Drawing Tools
- • Create Lines
- • Create Rectangles, Squares
- • Create Polygons/Circles
- • Create surfaces from lines, Circles and
- polygons
- • Triangulation
- • How SketchUp handles Curves
- • Freehand tool
- • Single and Multiple Selections
- 3D Geometry Construction Tools
- • Create 3-dimensional geometry
- • Create surfaces from lines in 3D
- • Demonstrate stickiness of geometry in
- 3D
- • Create geometry with the Push/Pull
- Tool
- • Push/Pull with Modifier Keys
- • Lock inferences
- Modification Tools
- • Move, Copy

- • Using Move to Resize Curves and
- Curved Surfaces
- • Rotate, Copy
- □ Defining the Rotation Axis
- □ Using Rotate to Twist
- • Scaling and Resizing
- • Offsetting Lines and faces
- • Follow Me
- □ Follow Me with Components
- □ Round Objects
- • Auto fold
- • Displaying and Smoothing Edges
- Making Multiple Copies
- • Internal Arrays
- • Non-Orthogonal Copies
- • Multiple Rotated Copies

- Groups and Components
- • The differences between Groups and
- Components
- • The importance of structuring your
- models with Groups and Components
- • Demonstration of Component
- inferencing behavior and
- characteristics
- • Creating and Saving Your Own
- Components
- • How to edit a Component
- • Removing Objects from a Group or
- Components
- • Scaling Components
- □ Aligning Components
- □ Resizing Components
- • Healing the edge of adjacent
- components
- • Work with the Components Browser
- □ Finding Components in the 3D
- Warehouse
- □ Opening the 3D Warehouse in Your
- Internet Browser
- □ Inserting and Editing Components

- Intersecting
- • Cutting
- • Arch Cutouts Using Groups
- • Intersect with Context and Selected
- Painting, Materials, and Textures
- • Applying Materials
- • Editing Materials
- • Using Images as Textures
- • Material Collections
- • Material Translucency
- • Double-Sided Faces
- • Materials of Groups and Components
- • Overview of Materials of Groups

h) Education Requirements
High School or higher

i) Course Level
Entry Level, Engineering

j) Method of Instruction
On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*
Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

CATIA Drafting Essentials (CAD-190)

This course explores CATIA V5. During this training students gain understanding of the CATIA V5 interface and how to use CATIAV5 to create solid models of parts, assemblies and drawings. Understand how to manage parts in the context of an assembly. A hands-on course where students produce simple parts drawings and assemblies

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

The SketchUp Workflow for Architecture: Modeling Buildings, Visualizing Design, and Creating Construction Documents with SketchUp Pro and LayOut, 1st Edition
by Michael Brightman (Author)

g) Course Outline

- Design Intent
- CATIA V5 User
- Introduction to CATIA
- Profile
- Multiple Profile Creation
- Sketch Constraints
- Basic Features Creation
- Edge and Face-Face Fillets
- Multiple Profile Sketch Features
- Sketch Analysis and Pocket
- Shaft and Groove
- Thin Pad and Shell
- Pad, Fillet, Hole and Shell
- Stiffeners and Draft
- Reflect Draft
- Thread and Tap
- Thread
- Features Deactivation
- Features Activation
- Update Error Management
- Dress-up Features
- Patterns
- Part Transformation and Catalog
- Patterns Modifications
- Pattern and Catalog
- Case Study: Reusing Data
- Material and Measures
- Parameter and Formula
- Finalizing Design Intent
- Basic Assembly Reuse Components
- Component Positioning
- Constrain Components
- Constraints Creation
- Degrees of Freedom
- Assembly Design
- Visualization and Design Modes
- Design in Context
- Drawing Creation

h) Education Requirements

High School or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

C Programming Essentials (CS-120)

This course teaches how to develop applications for mobile devices such as iPhones and iPads (iOS). We will go through the process of building a mobile application from start to finish using the iOS SDK (Software Development Kit). In lecture sessions, you will learn the basics of the Objective-C programming language, how to design mobile interfaces, how to use the libraries to build applications that have the proper look and feel, how to use table views, how to design and handle user input, and other aspects as time permits. During the lab sessions, students will create applications using the Xcode IDE (Integrated Development Environment).

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

The C Programming LanguageApr 1, 1988
by Brian W. Kernighan and Dennis M. Ritchie

g) Course Outline

•
Introduction to compiling and software development
- Basic scalar data types and their operators
- Flow control
- Complex data types: arrays, structures and pointers
- Structuring the code: functions and modules
- Preprocessing source code

Chapters:
Absolute basics
- languages: natural and artificial
- machine languages
- high-level programming languages
- obtaining the machine code: compilation process
- recommended readings
- your first program
- variable – why?
- integer values in real life and in “C”, integer literals

Data types
- floating point values in real life and in “C”, float literals
- arithmetic operators
- priority and binding
- post- and pre -incrementation and -decrementation
- operators of type op=
- char type and ASCII code, char literals
- equivalence of int and char data
- comparison operators
- conditional execution and if keyword
- printf() and scanf() functions: absolute basics

Flow control
- conditional execution continued: the “else” branch
- more integer and float types
- conversions – why?
- typecast and its operators
- loops – while, do and for
- controlling the loop execution – break and continue
- logical and bitwise operators

Arrays
- switch: different faces of ‘if’
- arrays (vectors) – why do you need them?
- sorting in real life and in a computer memory
- initiators: a simple way to set an array
- pointers: another kind of data in “C”
- an address, a reference, a dereference and the sizeof operator
- simple pointer and pointer to nothing (NULL)
- & operator
- pointers arithmetic
- pointers vs. arrays: different forms of the same phenomenon
- using strings: basics
- basic functions dedicated to string manipulation

Memory management and structures
- the meaning of array indexing
- the usage of pointers: perils and disadvantages
- void type
- arrays of arrays and multidimensional arrays
- memory allocation and deallocation: malloc() and free() functions
- arrays of pointers vs. multidimensional arrays
- structures – why?
- declaring, using and initializing structures
- pointers to structures and arrays of structures
- basics of recursive data collections

Functions
- functions – why?
- how to declare, define and invoke a function
- variables' scope, local variables and function parameters
- pointers, arrays and structures as function parameters
- function result and return statement
- void as a parameter, pointer and result
- parameterizing the main function
- external function and the extern declarator
- header files and their role

Files and streams
- files vs. streams: where does the difference lie?
- header files needed for stream operations
- FILE structure
- opening and closing a stream, open modes, errno variable
- reading and writing to/from a stream
- predefined streams: stdin, stdout and stderr
- stream manipulation: fgetc(), fputc(), fgets() and fputs() functions

- raw input/output: fread() and fwrite() functions

Preprocessor and complex declarations

- preprocessor – why?
- #include: how to make use of a header file
- #define: simple and parameterized macros
- #undef directive
- predefined preprocessor symbols
- macrooperators: # and ##
- conditional compilation: #if and #ifdef directives
- avoiding multiple compilations of the same header files
- scopes of declarations, storage classes
- user -defined types – why?
- pointers to functions
- analyzing and creating complex declarations

h) Education Requirements

The course does not assume prior knowledge of any specific topics, however a solid computer science foundation, and a reasonable amount of programming, as well as knowledge of basic computer science theory would be essential.

i) Course Level

Entry Level, Engineering

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

C++ PROGRAMMING ESSENTIALS (CS-140)

This course covers the C++ programming languages in detail. You will learn the required background knowledge, including memory management, pointers, preprocessor macros, object-oriented programming, and how to find bugs when you inevitably use any of those incorrectly. There will be daily assignments and an individual project.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

The C++ Programming Language, 4th Edition May 19, 2013 | Lay Flat
by Bjarne Stroustrup

g) Course Outline

- **SECTION 1: PERSPECTIVE**
  1. The Software Crisis
  2. Design Techniques
  3. Large Software Systems
  4. Roots of Object Technology
  5. What Is Object-Oriented Programming?
  6. C++ and Object-Oriented Programming
  7. Why C++?
  8. Features of C++
  9. Pros and Cons of C++
- **SECTION 2: THE LANGUAGE OF OBJECT-ORIENTATION**
  1. What Is an Object?
  2. What Is a Class?
  3. Encapsulation
  4. Data Hiding
  5. The Public Interface
  6. Relationships Among Classes
  7. Inheritance
  8. Polymorphism
  9. Object-Oriented Design
- **SECTION 3: C VS. C++**
  1. Comments
  2. Namespaces
  3. Simple Output
  4. Simple Input
  5. Definitions Near to First Use
  6. Function Prototypes
  7. The inline Specifier
  8. const
  9. Structure Members
  10. The Reference Type
  11. Overloading Function Names
  12. Default Parameters
  13. The Scope Resolution Operator
  14. Aggregates
  15. Operators new and delete
  16. The bool Data Type
  17. The string Data Type
- **SECTION 4: FUNDAMENTALS OF CLASSES**
  1. Data Types
  2. User Defined Data Types
  3. Using the Class Concept
  4. Defining a Class
  5. public and private Access Levels
  6. The Scope Resolution Operator ::
  7. Using Class Objects Like Built-in Types
  8. Scope
  9. Constructors
  10. Member Initialization Lists
  11. Destructors
  12. Array of Objects
  13. Pointers
  14. The this Pointer
  15. Passing Objects to Functions
  16. Returning Objects From Functions
  17. static Class Members
- **SECTION 5: OPERATOR OVERLOADING**
  1. Introduction
  2. Rules for Operator Overloading
  3. Rationale for Operator Overloading
  4. Overloading Member Functions
  5. Overloading Non-Member Functions
  6. friend Functions
  7. The Copy Constructor
  8. The Assignment Operator
  9. Overloading [ ]
  10. Overloading Increment and Decrement Operators
  11. const Objects and References
- **SECTION 6: COMPOSITION OF CLASSES**
  1. Relationships
  2. Composition of Classes
  3. The Point Class
  4. The Line Class
  5. Member Initialization Lists
  6. An Application With Composition

7. The Copy Constructor Under Composition
8. operator= Under Composition

- **SECTION 7: INHERITANCE**
  1. Introduction
  2. Public Base Classes
  3. The protected Access Level
  4. Member Initialization Lists
  5. What Isn't Inherited
  6. Assignments Between Base and Derived Objects
  7. Compile-Time vs. Run-Time Binding
  8. virtual Functions
  9. Polymorphism
  10. virtual Destructors
  11. Pure virtual Functions
  12. Abstract Base Classes
  13. An Extended Inheritance Example
- **SECTION 8: I/O IN C++**
  1. The iostream Library
  2. Predefined Streams
  3. Overloading operator<<
  4. Overloading operator>>
  5. Manipulators
  6. Stream States
  7. Formatted I/O
  8. Disk Files
  9. Reading and Writing Objects
- **SECTION 9: ADVANCED TOPICS**
  1. Template Functions
  2. Template Classes
  3. Multiple Inheritance
  4. User-Defined Conversions
  5. Data Structures
  6. An Iterator Class
  7. Exceptions
- **SECTION 10: INTRODUCTION TO THE STANDARD TEMPLATE LIBRARY**
  1. Introduction
  2. The Standard Template Library
  3. Design Goals
  4. STL Components
  5. Iterators
  6. Example: vector
  7. Example: list
  8. Example: set
  9. Example: map
  10. Example: find
  11. Example: merge
  12. Example: accumulate
  13. Function Objects
  14. Adaptors

h) Education Requirements

The course does not assume prior knowledge of any specific topics, however a solid computer science foundation, and a reasonable amount of programming, as well as knowledge of basic computer science theory would be essential.

i) Course Level

Entry Level, Engineering

j) Method of Instruction

Classroom style, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

HTML & CSS Essentials (CS-130)

Hands-on course in designing and developing Web pages using HTML (HyperText Markup Language) and CSS (Cascading Style Sheets). The course will cover HTML tags for text, images, links, lists, simple layouts, complex layouts, tables, frames, style, internal style sheets, and external style sheets. Basic issues in using graphics on the Web will also be covered.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Visual Quickstart Guide: HTML5 and CSS3 (7th edition) by Elizabeth Castro and Bruce Hyslop

g) Course Outline

- HTML skeleton
- HTML tags for text, links, lists
- HTML tags and web standards for images (graphics)
- Simple layouts
- Complex layouts
- HTML tags for layout
- HTML tags for tables
- HTML tags for styles
- Internal CSS style sheets
- External CSS style sheets
-

h) Education Requirements

The course does not assume prior knowledge of any specific topics, however a solid computer science foundation, and a reasonable amount of programming, as well as knowledge of basic computer science theory would be essential.

i) Course Level

Entry Level, Computer Science

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

JavaScript Essentials (CS-150)

Hands-on course in designing and developing Web pages using HTML (HyperText Markup Language) and CSS (Cascading Style Sheets). The course will cover HTML tags for text, images, links, lists, simple layouts, complex layouts, tables, frames, style, internal style sheets, and external style sheets. Basic issues in using graphics on the Web will also be covered.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Visual Quickstart Guide: HTML5 and CSS3 (7th edition) by Elizabeth Castro and Bruce Hyslop

g) Course Outline

- HTML skeleton
- HTML tags for text, links, lists
- HTML tags and web standards for images (graphics)
- Simple layouts
- Complex layouts
- HTML tags for layout
- HTML tags for tables
- HTML tags for styles
- Internal CSS style sheets
- External CSS style sheets
-

h) Education Requirements

The course does not assume prior knowledge of any specific topics, however a solid computer science foundation, and a reasonable amount of programming, as well as knowledge of basic computer science theory would be essential.

i) Course Level

Entry Level, Computer Science

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

JAVA PROGRAMMING ESSENTIALS (CS-155)

This course teaches students how to develop Java applications. Topics covered include the Java programming language syntax, OO programming using Java, exception handling, file input/output, threads, collection classes, and networking. Students will develop and test Java applications (typically) using Eclipse.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Head First Java, 2nd Edition Feb 9, 2005, by Kathy Sierra and Bert Bates

g) Course Outline

- Compile and run a Java application.
- Understand the role of the Java Virtual Machine in achieving platform independence.
- Navigate through the API docs.
- Use the Object Oriented paradigm in Java programs.
- Understand the division of classes into Java packages.
- Use Exceptions to handle run time errors.
- Select the proper I/O class among those provided by the JDK.
- Use threads in order to create more efficient Java programs.

h) Education Requirements

Students should have taken the Software Development for Non-Programmers course or have programmed in at least one programming language - preferably C or C++. Some familiarity with Object Oriented Programming is desired but not required.

i) Course Level

Entry Level, Computer Science

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

PHP/MYSQL ESSENTIALS (CS-160)

This course explores integrated suite of open source technologies: PHP and MySQL. During the course students learn how integrate them into a dynamic, data-driven web site.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

PHP and MySQL Web Development (4th Edition) 4th Edition
by Luke Welling (Author), Laura Thomson (Author)

g) Course Outline

- Creating and modifying a PHP page
- Working with variables and data types
- Using if/elseif/else statements to control processing conditionally
- Creating programs that include for, while, and do loops to process statements repeatedly
- Employing the break, continue, and exit statements to modify default loop behaviors
- Creating arrays
- How to manipulate strings in PHP using the built-in functions
- Maintaining state using cookies, session variables, hidden form fields and query strings
- The fundamental techniques necessary to create a shopping cart solution
- Using SQL to SELECT, INSERT, UPDATE and DELETE data from tables
- Using the phpMyAdmin utility to administer the MySQL database
- Using PHP to manipulate files
- To identify and handle the three main types of errors that can occur when programming with PHP

h) Education Requirements

Experience with at least one programming language. Ability to create a web page using HTML

i) Course Level

Entry Level, Computer Science

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:

Python Programming Essentials (CS-165)

This course introduces the student to the Python language. Upon completion of this class, the student will be able to write non trivial Python programs dealing with a wide variety of subject matter domains. Topics include language components, the IDLE environment, control flow constructs, strings, I/O, collections, classes, modules, and regular expressions. The course is supplemented with many hands on labs using either Linux or Windows.

d) Length of program:

The course duration is 12 weeks.

e) Class Sessions

Classes are being held twice a week, typically 3 hours each.

f) Text Books

Learning Python, 5th Edition
by Mark Lutz

g) Course Outline

Describe the basic elements of the Python language and the Python interpreter and discuss the differences between Python and other modern languages.
• Analyze and demonstrate the use of lists and tuples in Python.
• Describe and use Python dictionaries correctly and demonstrate the use of dictionary methods.
• Define, analyze and code the basic Python conditional and iterative control structures and explain how they can be nested and how exceptions can be used.
• Design, implement, test, and debug functions and methods that can be used in programs, and demonstrate the way parameters are passed in such functions and methods.
• Write classes to demonstrate the ideas of encapsulation, inheritance, interfaces and object oriented program design.
• Explain and demonstrate methods of error handling and Python exceptions.
• Demonstrate the understanding of "magic methods" through use of these in the context of a Python application.
• Use pre-written modules and learn the techniques necessary for creating modules.
• Write to and read from files using intermediate file I/O operations in a Python program.
• Use an existing library to implement a graphical user interface
• Design, implement, test, and debug a program that uses each of the following fundamental programming constructs: string processing, numeric computation, simple I/O, arrays and the Python standard library.
• Solve problems that have origins in a variety of disciplines including math, science, the Internet and business.

h) Education Requirements

Experience with at least one programming language.

i) Course Level

Entry Level, Computer Science

j) Method of Instruction

On Campus, combinations of lecture and hand-on computer lab

k*) Clock Hours*

Total instructional Clock Hour is 120 consisting of 48 hours of lecture and 72 hours of computer Lab

a) Course Title:
VLSI Physical Design Essentials (EE-220)

b) Objectives
This course is structured to enable students to acquire an in-depth knowledge of all aspects of Physical design, from Netlist to GDSII including Floor planning, Placement, power planning, scan chain reordering, global routing, clock tree synthesis, power analysis and ECO. Course includes several hands-on projects.

d) Length of program
The course duration is 24 weeks long.

e) Class Sessions
Classes are being two sessions per week, typically 3 hours each.

f) Textbooks
VLSI Physical Design: From Graph Partitioning to Timing Closure
by Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu
Publisher: Springer; 2011 edition (February 9, 2011)
Language: English
ISBN-10: 904819590X
ISBN-13: 978-9048195909

g) Course Outline

- Introduction to physical design automation
- Floor planning and Placement
- Grid Routing and Global Routing
- Detailed Routing and Clock Design
- Clocking Issues and Clock Tree Design
- Static Timing Analysis
- Static Timing Analysis (contd.)
- Signal Integrity and Crosstalk Issues
- Low Power Design Issues
- Low Power Design Techniques and Planning
- Layout Compaction and Miscellaneous Problems
- Physical Verification and Sign-off

h) Education Requirements
BSEE or higher

i) Course Level
Entry Level, Engineering

j) Method of Instruction
On Campus, combinations of lecture and class assignments

k) Clock Hours
Total instructional Clock Hour is 160 consisting of 96 hours of lecture and 64 hours of projects and assignments.

a) Course Title:
Professional Scrum Developer (SM-130)

b) Objectives
During this training students gain both a theoretical and a real-world view of what it is like to build software with Scrum. Throughout the course, students collaborate together as a team in a series of Sprints where they apply modern engineering practices, and use the Scrum framework to cope with changes. There is a key focus on having students learn how to develop increments of potentially releasable functionality from a realistic Product Backlog. Students who complete the course will be prepared to take the Professional Scrum Developer (PSD) professional certification examination.

d) Length of program
The course duration is 6 weeks long.

e) Class Sessions
Classes are being two sessions per week typically 4 hours each.

f) Textbooks
A Guide to Scrum Developer
by Devsena Mishra
Publisher: CreateSpace Independent Publishing Platform; 1 edition (November 29, 2015)
ISBN-10: 151960873X
ISBN-13: 978-1519608734

g) Course Outline
Introduction of Agile – Why Agile, Agile Manifesto, Agile principles and values
Introduction of Other Agile Methodologies – XP, Kanban, Lean and DSDM
Scrum Framework – Scrum Roles, Scrum Ceremonies and Scrum Artifacts
Estimation and Planning – User Story writing and Estimation techniques
Distributed Team and best practices for distributed team
Introduction to Acceptance Test Driven Development
Behavior Driven Development – why, what and how
Difference between ATDD, BDD and TDD
Hands-on practice on Fitnesse, Cucumber, Selenium and SpecFlow
Planning Agile Software Development
Agile Architecture and Design
SOLID design Principles
Test Driven Development
Mocking
Refactoring, Patterns and Anti-Patterns
When and how to Refactor
Collaboration and Pair Programming
Continuous Integration
How to use TDD with Continuous Integration

h) Education Requirements
AA or higher

i) Course Level
Entry Level, Engineering

j) Method of Instruction
On Campus, combinations of lecture and class assignments

k) Clock Hours

Total instructional Clock Hour is 60 consisting of 48 hours of lecture and 12 hours of projects and assignments.

a) Course Title:
Professional Scrum Master Level II (SM-125)

b) Objectives
This training prepares the students to take Scrum Master II certification test. Students should have advanced Scrum knowledge, in-depth Scrum experience and/or have taken the Professional Scrum Master course prior to taking this assessment. However, attending a course is neither necessary nor sufficient for certification. The PSM II assessment consists of multiple-choice questions based on your knowledge of Scrum and how you would handle real-world situations.

d) Length of program
The course duration is 6 weeks long.

e) Class Sessions
Classes are being two sessions per week typically 4 hours each.

f) Textbooks
There are no textbooks for this training. Course handouts will be provided to students free of charge.

g) Course Outline
- Scrum theory and principles
- The Scrum Framework
- The Definition of Done
- Running a Scrum project
- Working with people and teams
- Scrum in your organization
- The role of the Scrum Master

h) Education Requirements
BSEE/BSCS/BA or higher

i) Course Level
Entry Level, Engineering

j) Method of Instruction
On Campus, combinations of lecture and class assignments

k) Clock Hours
Total instructional Clock Hour is 60 consisting of 48 hours of lecture and 12 hours of team projects and assignments.

a) Course Title:
Automated Software Testing with Selenium IDE (CS-175)

b) Objectives
Selenium IDE is one of the most popular test automation integrated development environments. This course students from basics to advance level in a very effective manner. Students do not need to have any prior programming skills or deep knowledge about software testing before taking this course. The basics are well covered in this course and gradually the course takes to advance levels.

d) Length of program
The course duration is 12 weeks long.

e) Class Sessions
Classes are being one session per week typically 3 hours each.

f) Textbooks
Selenium 2 Testing Tools: Beginner's Guide, by David Burns(Author)
Publisher: Packet Publishing (October 19, 2012)
ISBN-10: 1849518300
ISBN-13: 978-1849518307

g) Course Outline

1. Introduction to Automation
   a. What is automation testing
   b. Advantages of automation testing
   c. How to learn automation tool
2. Introduction of Selenium IDE
   a. Selenium IDE installation steps
   b. Understanding of Selenium IDE Toolbar Components
   c. Recording sample script in Selenium IDE with Examples
3. Selenium IDE Actions Commands
   a. Select commands with examples in Selenium IDE
   b. Mouse related commands with examples in Selenium IDE
4. Selenium IDE Assertions Commands to verify
   a. Verification commands with examples Selenium IDE
   b. Assertion commands with examples Selenium IDE
   c. Wait for commands with examples in Selenium IDE
5. Accessors commands
   a. Store commands with examples in Selenium IDE
   b. Keyboard commands with examples in Selenium IDE
6. Building Test cases
   a. Running test cases in FireFox
   b. Recording, playing back and saving the test script
   c. Using Base URL to run test cases in different domains
   d. Using Test Suites
7. Advanced topics to work on Selenium IDE
   a. How to use JavaScript in Selenium IDE
   b. Using plugins with Selenium IDE◦ Managing product end of life

h) Education Requirements
AA or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction
On Campus, combinations of lecture and class assignments

k) Clock Hours
Total instructional Clock Hour is 60 consisting of 18 hours of lecture and 42 hours of projects and assignments.

a) Course Title:
Custom Physical Design Essentials (EE-215)

b) Objectives
this course introduces the students to the process, tools and methodology of IC Layout Design and Verification using the latest Design Automation tools. The course provides the students with the insight into the exciting field of semiconductor technology and electronic devices, and trains them in IC layout techniques for a variety of application in Digital, Analog, and RFIC. This training program prepares students for entry-level positions in the industry.

d) Length of program
The course duration is 24 weeks long.

e) Class Sessions
Classes are being two sessions per week, typically 3 hours each.

f) Textbooks
This course does not have any textbook. Handout will be provided to students free of charge.

g) Course Outline

- Introduction & Outline
- Key Terminologies and Definitions
- Process Overview
- Materials Properties, Physical
- Materials Properties, Electrical
- Conductors, Insulators, Semiconductors
- Silicon Properties
- Silicon Wafer, Making of
- Crystal Orientation
- Electrons and Holes
- Semiconductor Types and Properties
- Sample Fabrication Flow
- Transistor Descriptions and Types
- Device Scaling
- Technology Nodes
- Topological Design Rules
- Electrical Design Rules
- IC Design Flows, Digital, Analog, Mixed Signal
- Analysis of Layout Rules
- Overview of Layout Tools
- Layout Examples and Assignments
- Electrical Conduction
- Current Flow
- Electric Force, Voltage Field
- Conductivity and Resistivity
- Resistance and Ohms Law
- Resistivity of Materials
- Discrete Resistors
- Integrated Resistors
- Poly Resistor Layout
- Sheet Resistivity
- Resistor Equations
- Parallel and Series Resistors
- Poly Resistor Assignments
- Serpentine Resistors
- Narrow Resistors
- Contact Placements
- Salicide and Block Layer
- Layout Implementation
- Poly Resistor Assignments
- N-Well Resistors
- Applications
- N-Well Resistors Layout Assignments
- N+ Resistors
- N+ Resistors Layout Assignments
- Thin-Film Resistors
- Laser Trimming
- Thin-Film Resistors Layout Assignments
- Comparing IC Resistors
- Resistor Models
- Parasitic Components
- Capacitors
- Capacitor Equations
- Capacitors and Energy
- Series and Parallel Capacitors
- Capacitors and Circuits
- Capacitors; Power and Delay Equations
- Discrete Capacitors
- IC Capacitors
- Metal to Metal, Poly to Metal, Stack
- Poly to Silicon Capacitors
- Analog Capacitor Modules
- Lateral Flux Capacitors
- Woven Lateral Flux Capacitors
- Layout issues in capacitors
- Inductors
- Inductor Equations
- Inductors and Energy
- Inductors and Circuits
- Discrete Inductors
- Quality Factor
- IC Inductors
- Inductors Importance in Design
- Inductor Layouts
- Inductor Models
- Substrate Loss
- Various Inductor Layouts
- Shielding Inductors
- Inductor Layout Assignments
- Pcells
- Wirebond Inductors
- IC Transformers
- Asymmetric, Symmetric, and Balanced Transformers
- Transformer Layout Assignments
- Active Semiconductor Devices (Diodes, Transistors)
- PN Junction and Diode Fundamentals
- Diode Applications
- Diode Layout Description
- Diode Applications in IC
- Transistor Fundamentals
- Transistor Applications
- MOS Transistor Fundamentals
- Bipolar Transistor Fundamentals
- FinFET Transistor
- Transistor Cross Section & Layout
- Well and Substrate Tap
- Parallel and Series Transistors
- Diffusion Merging
- Transistor Folding
- Finger & Bent Gates
- Transistor Layout Assignments
- Device Matching Principles
- Mismatch Definition
- Measuring Mismatch
- Importance of Matching
- Systematic and Random Mismatch
- Factors Causing Mismatch
- Methods for Reducing Mismatch
- Resistor Matching Guidelines
- Resistor Matching Assignment
- Capacitor Matching Guidelines
- Capacitor Matching Assignments
- Transistor matching issues
- Transistor matching techniques
- Cross coupled pairs

Analog building blocks
Schematic analysis and physical implementation of:
Current mirrors, differential amplifiers, voltage references
Analog Layout assignments
Parasitic components of devices
Methods for shielding devices and interconnect from noise sources
Noise isolation techniques
Latch-up description
Latch-up prevention techniques
Strapping & guard-ring techniques
IR drop and prevention methods
Power Supply networks
Device Isolation schemes
Electromigration overview and layout guidelines
Antenna phenomena & layout solutions
ESD & peripheral output driver layout techniques
Stick diagrams
Standard Cells
Standard cell library development
Bonding pad, seal-ring, scribe-line layout techniques
Power bus routing, bus slotting, & clock net routing techniques
Design and Verifications Flows
Review key design rules (such as 0.35nm, 0.25nm, 0.18nm, 14nm)
Technology review of advanced Semiconductor technology such as FINFET, etc.
Design Rule versus Process
Overview of Analog Layout Methods
Review of DRC files
DRC Flow
LVS Flow
Boolean Operations
DRC Rule File Creation
Identify DRC Errors
Manufacturability Rules
PDK Review
Schematic Creation
Symbol creation
Using PDK in layout development
Identify and Fix LVS Errors
Various Real Industry Projects
Calibre Training

h) Education Requirements
AA or higher

i) Course Level
Entry Level, Engineering

j) Method of Instruction
On Campus, combinations of lecture and class assignments

k) Clock Hours
Total instructional Clock Hour is 240 consisting of 144 hours of lecture and 96 hours of projects and assignments.

a) Course Title:
Full Stack Software Development Essentials (CS-170)

b) Objectives
In this training program, students are thought two full stacks, consisting of front-end, Back-end, and database, to help ensure that you are prepared to work at every different level of the development process—from front-end to back-end to data storage. Course curriculum is designed to provide the students the versatility they need to land that dream job as a software developer.

d) Length of program
The course duration is 10 weeks long.

e) Class Sessions
Classes are being held daily, Monday through Friday from 8am to 5pm.

f) Textbooks
There are no textbooks for this training. Course handouts will be provided to students free of charge.

g) Course Outline
- Web Fundamentals
- Python stack essentials
- MEAN stack essentials

h) Education Requirements
BSEE/BSCS or higher

i) Course Level
Entry Level, Engineering

j) Method of Instruction
On Campus, combinations of lecture and hand-on computer lab

k) Clock Hours
Total instructional Clock Hour is 400 consisting of 100 hours of lecture and 300 hours of computer Lab

a) Course Title:
Digital Manufacturing & Industry 4.0 Essentials (ME-200)

b) Objectives
This training provides a comprehensive overview of the digital manufacturing for Industry 4.0. The course examines the key technological advances that form the pillars of Industry 4.0 and explores their potential technical and economic benefits using examples of real-world applications. The changing dynamics of global production, such as more complex and automated processes, high-level competitiveness and emerging technologies, have paved the way for a new generation of goods, products and services. Moreover, manufacturers are increasingly realizing the value of the data that their processes and products generate. Such trends are transforming manufacturing industry to the next generation, namely Industry 4.0, which is based on the integration of information and communication technologies and industrial technology.

d) Length of program
The course duration is 12 weeks long.

e) Class Sessions
Classes are being two sessions per week typically 2 hours each.

f) Textbooks
Industry 4.0: Managing the Digital Transformation
by Alp Ustundag and Emre Cevikcan
Publisher: Springer; 1st ed. 2018 edition (September 15, 2017)
ISBN-10: 3319578693
ISBN-13: 978-3319578699

g) Course Outline
A Conceptual Framework for Industry 4.0
Smart and Connected Product Business Models
Lean Production Systems for Industry 4.0
Maturity and Readiness Model for Industry 4.0 Strategy
Technology Roadmap for Industry 4.0
Project Portfolio Selection for the Digital Transformation Era
Talent Development for Industry 4.0
The Changing Role of Engineering Education in Industry 4.0 Era
Data Analytics in Manufacturing
Internet of Things and New Value Proposition
Advances in Robotics in the Era of Industry 4.0
The Role of Augmented Reality in the Age of Industry 4.0
Additive Manufacturing Technologies and Applications
Advances in Virtual Factory Research and Applications
Digital Traceability Through Production Value Chain
Overview of Cyber Security in the Industry 4.0 Era

h) Education Requirements
AA or higher

i) Course Level

Entry Level, Engineering

j) Method of Instruction
On Campus, combinations of lecture and class assignments

k) Clock Hours
Total instructional Clock Hour is 120 consisting of 72 hours of lecture and 48 hours of projects and assignments.

a) Course Title:
Product Management Essentials (EM-130)

b) Objectives
This class is designed for everyone who is new to product management. The program covers everything from ideation to product end of life. It is the most comprehensive program that product managers can use to be effective from day one.

d) Length of program
The course duration is 6 weeks long.

e) Class Sessions
Classes are being two sessions per week typically 4 hours each.

f) Textbooks
There are no textbooks for this training. Course handouts will be provided to students free of charge.

g) Course Outline

Introduction
- What is a product?
- What is product management?
- How is it different from project management?

The product Manager:
- What does a product manager do?
- How do organizations affect the role?
-

Product Ideation
- Ideation techniques
- Ideation Case study

Exploring:
- Sensing [Market and competitor analysis]
- Seizing [Portfolio Planning, Segmenting and Targeting]

Pricing
- Basics of pricing
- Pricing techniques

Defining the product
- What is re-framing
- What is innovation.
- The innovation cycle
- Idea refinement
- Tools for idea refinement

Business case
- What is a business case and why do we need it?
- Creating a business case

Technical implementation
- Feature planning and prioritization
- Execution
- Pilot
- A/B testing

Product Launch
- Factors to consider during the launch
- Key points for a successful launch

Product life cycle and end of life planning
- The product life cycle curve
- Factors affecting the product lifecycle
- Reasons for product end of life.
- Factors to consider for end of life *planning*
- Managing product end of life

h) Education Requirements
AA or higher

i) Course Level
Entry Level, Engineering

j) Method of Instruction
On Campus, combinations of lecture and class assignments

k) Clock Hours
Total instructional Clock Hour is 60 consisting of 48 hours of lecture and 12 hours of team projects and assignments.

APPENDIX –II

Listing of programs offered by Silicon Valley Polytechnic Institute, Inc.

No.	Course	Duration (Weeks)	Clock Hours	Tuition	Registration Fee	Materials Fee	*STRF Fee	**Program Total Charges
1	3D MICROELECTRONIC SYSTEM INTEGRATION	12	120	$3000	$150	0	$7.50	$3,157.50
2	ADVANCED 3D COMPUTER AIDED DESIGN AND DRAFTING WITH SOLIDWORKS	12	120	$3000	$150	0	$7.50	$3,157.50
3	ADVANCED ANALOG CMOS IC DESIGN	12	120	$3000	$150	0	$7.50	$3,157.50
4	ADVANCED AND 3D COMPUTER DRAFTING AND DESIGN WITH AUTOCAD	12	120	$3000	$150	0	$7.50	$3,157.50
5	ADVANCED PCB LAYOUT DESIGN	12	120	$3000	$150	0	$7.50	$3,157.50
6	ADVANCED RFIC DESIGN	12	120	$3000	$150	0	$7.50	$3,157.50
7	ADVANCED SEMICONDUCTOR DEVICES - PHYSICS & TCAD	12	120	$3000	$150	0	$7.50	$3,157.50
8	ADVANCED SEMICONDUCTOR TECHNOLOGY AND FABRICATION	12	120	$3000	$150	0	$7.50	$3,157.50
9	ADVANCED SOLAR PHOTOVOLTAIC SYSTEM DESIGN	12	120	$3000	$150	0	$7.50	$3,157.50
10	APPLIED ELECTRICITY AND ELECTRONICS FUNDAMENTALS	12	120	$3000	$150	0	$7.50	$3,157.50
11	AUTODESK REVIT ARCHITECTURE ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
12	AUTOMATED SOFTWARE TESTING WITH SELENIUM IDE	12	120	$3000	$150	0	$7.50	$3,157.50
13	AUTOMATED TEST AND MEASUREMENT WITH LABVIEW	12	120	$3000	$150	0	$7.50	$3,157.50
14	C PROGRAMMING ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
15	C++ PROGRAMMING ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
16	CATIA DRAFTING ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
17	COMPUTER AIDED DESIGN AND DRAFTING WITH AUTOCAD	12	120	$3000	$150	0	$7.50	$3,157.50
18	COMPUTER AIDED DESIGN AND DRAFTING WITH SOLIDWORKS	12	120	$3000	$150	0	$7.50	$3,157.50
19	COMPUTER AND NETWORK SECURITY ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
20	COMPUTER NETWORKING FUNDAMENTALS	12	120	$3000	$150	0	$7.50	$3,157.50
21	CUSTOM PHYSICAL DESIGN ESSENTIALS	16	160	$6000	$150	0	$15.00	$6,165.00
22	CYBERSECURITY FOUNDATIONS	12	120	$3000	$150	0	$7.50	$3,157.50
23	CYBERSECURITY IMPLEMENTATION	12	120	$3000	$150	0	$7.50	$3,157.50
24	DESIGN OF ANALOG CMOS INTEGRATED CIRCUITS	12	120	$3000	$150	0	$7.50	$3,157.50
25	DESIGN OF DIGITAL CMOS INTEGRATED CIRCUITS	12	120	$3000	$150	0	$7.50	$3,157.50
26	DESIGN OF LOW POWER DIGITAL INTEGRATED CIRCUITS	12	120	$3000	$150	0	$7.50	$3,157.50
27	DESIGN OF RADIO FREQUENCY INTEGRATED (RFIC) CIRCUITS	12	120	$3000	$150	0	$7.50	$3,157.50
28	DESIGN SIGNAL PROCESSING PRINCIPLES AND APPLICATIONS	12	120	$3000	$150	0	$7.50	$3,157.50
29	DIGITAL LOGIC DESIGN FUNDAMENTALS	12	120	$3000	$150	0	$7.50	$3,157.50
30	DIGITAL MANUFACTURING & INDUSTRY 4.0 ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
31	DIGITAL SIGNAL PROCESSING WITH MATLAB	12	120	$3000	$150	0	$7.50	$3,157.50
32	DIGITAL VLSI IC DESIGN WITH VERILOG	12	120	$3000	$150	0	$7.50	$3,157.50
33	EMBEDDED SYSTEM DESIGN FUNDAMENTALS	12	120	$3000	$150	0	$7.50	$3,157.50
34	FPGA DESIGN FUNDAMENTALS	12	120	$3000	$150	0	$7.50	$3,157.50
35	FULL STACK SOFTWARE DEVELOPMENT ESSENTIALS	10	400	$6000	$150	0	$15.00	$6,165.00
36	HTML & CSS ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
37	IC LAYOUT DESIGN	12	120	$3000	$150	0	$7.50	$3,157.50
38	IC LAYOUT VERIFICATION	12	120	$3000	$150	0	$7.50	$3,157.50
39	IC PACKAGING DESIGN ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
40	IC PACKAGING FUNDAMENTALS	12	120	$3000	$150	0	$7.50	$3,157.50
41	INTERNET OF THINGS (IOT) DESIGN & APPLICATION	12	120	$3000	$150	0	$7.50	$3,157.50
42	INTERNET OF THINGS (IOT) FUNDAMENTALS	12	120	$3000	$150	0	$7.50	$3,157.50
43	JAVA PROGRAMMING ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
44	JAVASCRIPT ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
45	LOW POWER VLSI DESIGN	12	120	$2000	$150	0	$5.00	$2,155.00
46	MATLAB FOR ENGINEERING AND SCIENTIFIC APPLICATIONS	12	120	$3000	$150	0	$7.50	$3,157.50
47	MECHANICAL DRAFTING FUNDAMENTALS	12	120	$3000	$150	0	$7.50	$3,157.50
48	MEM DESIGN & TECHNOLOGY FUNDAMENTALS	12	120	$3000	$150	0	$7.50	$3,157.50
49	NATIONAL ELECTRICAL CODE (NEC) TRAINING	12	120	$3000	$150	0	$7.50	$3,157.50
50	PCB AND PWB TECHNOLOGY FUNDAMENTALS	12	120	$3000	$150	0	$7.50	$3,157.50
51	PCB LAYOUT DESIGN	12	120	$3000	$150	0	$7.50	$3,157.50
52	PHP/MYSQL PROGRAMMING ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
53	PHYTON PROGRAMMING ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
54	PRACTICAL DESIGN WITH DSP	12	120	$3000	$150	0	$7.50	$3,157.50
55	PRODUCT MANAGEMENT ESSENTIALS	6	60	$3000	$150	0	$7.50	$3,157.50
56	PROFESSIONAL SCRUM DEVELOPER	6	60	$3000	$150	0	$7.50	$3,157.50
57	PROFESSIONAL SCRUM MASTER LEVEL II	6	60	$3000	$150	0	$7.50	$3,157.50

* Effective April 1, 2022, the Student Tuition Recovery Fund (STRF) assessment rate is two dollars and fifty cents ($2.50) per one thousand dollars ($1,000) of institutional charges.

**This represents the schedule of total charges for a period of attendance AND estimated schedule of total charges for the entire educational program. The amount is due and must be paid prior to the start of training.

APPENDIX –II – Continued from previous page

Listing of programs offered by Silicon Valley Polytechnic Institute, Inc.

No.	Course	Duration (Weeks)	Clock Hours	Tuition	Registration Fee	Materials Fee	*STRF Fee	** Total Charges
58	PROJECT MANAGEMENT ESSENTIALS	6	60	$3000	$150	0	$7.50	$3,157.50
59	REVIT ARCHITECTURE COMMERCIAL AND MEP	12	120	$3000	$150	0	$7.50	$3,157.50
60	SCRUM MASTER AND JIRA TRAINING	6	60	$3000	$150	0	$7.50	$3,157.50
61	SCRUM MASTER BOOTCAMP	2 days	14	$2000	$150	0	$5.00	$2,155.00
62	SKETCHUP ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
63	SOFTWARE QUALITY ASSURANCE ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
64	SOLAR PHOTOVOLTAIC DEVICE PHYSICS	12	120	$3000	$150	0	$7.50	$3,157.50
65	SOLAR PHOTOVOLTAIC SYSTEM DESIGN ESSENTIALS	12	120	$3000	$150	0	$7.50	$3,157.50
66	TIMING VERIFICATION OF DIGITAL VLSI DESIGNS	12	120	$3000	$150	0	$7.50	$3,157.50
67	VLSI PHYSICAL DESIGN ESSENTIALS	16	160	$6000	$150	0	$15.00	$6,165.00

* Effective April 1, 2022, the Student Tuition Recovery Fund (STRF) assessment rate is two dollars and fifty cents ($2.50) per one thousand dollars ($1,000) of institutional charges.

**This represents the schedule of total charges for a period of attendance AND estimated schedule of total charges for the entire educational program. The amount is due and must be paid prior to the start of training.

APPENDIX –III – SOCO Codes

SOCO Codes for Programs offered by Silicon Valley Polytechnic Institute, Inc.

No.	Course	SOCO
1	3D MICROELECTRONIC SYSTEM INTEGRATION	17-2060
2	ADVANCED 3D COMPUTER AIDED DESIGN AND DRAFTING WITH SOLIDWORKS	17-3011
3	ADVANCED ANALOG CMOS IC DESIGN	17-2060
4	ADVANCED AND 3D COMPUTER DRAFTING AND DESIGN WITH AUTOCAD	17-2060
5	ADVANCED PCB LAYOUT DESIGN	17-2060
6	ADVANCED RFIC DESIGN	17-2060
7	ADVANCED SEMICONDUCTOR DEVICES - PHYSICS & TCAD	17-2060
8	ADVANCED SEMICONDUCTOR TECHNOLOGY AND FABRICATION	17-2060
9	ADVANCED SOLAR PHOTOVOLTAIC SYSTEM DESIGN	17-2060
10	APPLIED ELECTRICITY AND ELECTRONICS FUNDAMENTALS	17-2060
11	AUTODESK REVIT ARCHITECTURE ESSENTIALS	17-2060
12	AUTOMATED SOFTWARE TESTING WITH SELENIUM IDE	17-2060
13	AUTOMATED TEST AND MEASUREMENT WITH LABVIEW	17-2060
14	C PROGRAMMING ESSENTIALS	15-1131
15	C++ PROGRAMMING ESSENTIALS	15-1131
16	CATIA DRAFTING ESSENTIALS	17-2060
17	COMPUTER AIDED DESIGN AND DRAFTING WITH AUTOCAD	17-3011
18	COMPUTER AIDED DESIGN AND DRAFTING WITH SOLIDWORKS	17-3011
19	COMPUTER AND NETWORK SECURITY ESSENTIALS	17-2060
20	COMPUTER NETWORKING FUNDAMENTALS	17-2060
21	CUSTOM PHYSICAL DESIGN ESSENTIALS	17-2060
22	CYBERSECURITY FOUNDATIONS	17-2060
23	CYBERSECURITY IMPLEMENTATION	17-2060
24	DESIGN OF ANALOG CMOS INTEGRATED CIRCUITS	17-2060
25	DESIGN OF DIGITAL CMOS INTEGRATED CIRCUITS	17-2060
26	DESIGN OF LOW POWER DIGITAL INTEGRATED CIRCUITS	17-2060
27	DESIGN OF RADIO FREQUENCY INTEGRATED (RFIC) CIRCUITS	17-2060
28	DESIGN SIGNAL PROCESSING PRINCIPLES AND APPLICATIONS	17-2060
29	DIGITAL LOGIC DESIGN FUNDAMENTALS	17-2060
30	DIGITAL MANUFACTURING & INDUSTRY 4.0 ESSENTIALS	17-2060
31	DIGITAL SIGNAL PROCESSING WITH MATLAB	17-2060
32	DIGITAL VLSI IC DESIGN WITH VERILOG	17-2060
33	EMBEDDED SYSTEM DESIGN FUNDAMENTALS	17-2060
34	FPGA DESIGN FUNDAMENTALS	17-2060
35	FULL STACK SOFTWARE DEVELOPMENT ESSENTIALS	15-1131
36	HTML & CSS ESSENTIALS	15-1131
37	IC LAYOUT DESIGN	17-3012
38	IC LAYOUT VERIFICATION	17-3012
39	IC PACKAGING DESIGN ESSENTIALS	17-2060
40	IC PACKAGING FUNDAMENTALS	17-2060
41	INTERNET OF THINGS (IOT) DESIGN & APPLICATION	17-2060
42	INTERNET OF THINGS (IOT) FUNDAMENTALS	17-2060
43	JAVA PROGRAMMING ESSENTIALS	15-1131
44	JAVASCRIPT ESSENTIALS	15-1131
45	LOW POWER VLSI DESIGN	17-2060
46	MATLAB FOR ENGINEERING AND SCIENTIFIC APPLICATIONS	17-2060
47	MECHANICAL DRAFTING FUNDAMENTALS	17-3024
48	MEM DESIGN & TECHNOLOGY FUNDAMENTALS	17-2060
49	NATIONAL ELECTRICAL CODE (NEC) TRAINING	17-2060
50	PCB AND PWB TECHNOLOGY FUNDAMENTALS	17-2060
51	PCB LAYOUT DESIGN	17-3012
52	PHP/MYSQL PROGRAMMING ESSENTIALS	15-1131
53	PHYTON PROGRAMMING ESSENTIALS	15-1131
54	PRACTICAL DESIGN WITH DSP	17-2060
55	PRODUCT MANAGEMENT ESSENTIALS	13-1082
56	PROFESSIONAL SCRUM DEVELOPER	13-1082
57	PROFESSIONAL SCRUM MASTER LEVEL II	13-1082

APPENDIX –III – Continued from previous page
SOCO Codes for Programs offered by Silicon Valley Polytechnic Institute, Inc.

No.	Course	SOCO
58	PROJECT MANAGEMENT ESSENTIALS	13-1082
59	REVIT ARCHITECTURE COMMERCIAL AND MEP	17-3011
60	SCRUM MASTER AND JIRA TRAINING	13-1082
61	SCRUM MASTER BOOTCAMP	13-1082
62	SKETCHUP ESSENTIALS	17-3011
63	SOFTWARE QUALITY ASSURANCE ESSENTIALS	15-1131
64	SOLAR PHOTOVOLTAIC DEVICE PHYSICS	47-2111
65	SOLAR PHOTOVOLTAIC SYSTEM DESIGN ESSENTIALS	47-2111
66	TIMING VERIFICATION OF DIGITAL VLSI DESIGNS	17-2060
67	VLSI PHYSICAL DESIGN ESSENTIALS	17-2060

APPENDIX –IV
Listing and qualification of SVPTI Faculty

Faculty Name: Dr. Sunil Mehta

1. **Educational Background:**
    a. **Earned Degree: Ph.D. in EE**
    b. **Name of the Institution awarding the above Degree: Stanford University**
    c. **Date degree was granted: June 1988**
2. **Fields of specialization: Computer Science**

3. **Teaching, research and, administrative experience: Over 28 years of experience in high-tech industry in area of electronic design.**

4. **Teaching assignments:**

    Full Stack Program Development Essentials
    Automated Software Testing with Selenium IDE

Faculty Name: Dr. Rahul Shringarpure

1. **Educational Background:**
    a. **Earned Degree: Ph.D. in EE**
    b. **Name of the Institution awarding the above Degree: Arizona State University**
    c. **Date degree was granted: June 2008**
2. **Fields of specialization: Electronic Design**

3. **Teaching, research and, administrative experience: Over 7 years of experience in high-tech industry in area of electronic design.**

4. **Teaching assignment:**

    VLSI Physical Design Essentials

Faculty Name: Dr. Kris Verma

1. **Educational Background:**

    a. **Earned Degree: Ph.D. in EE**
    b. **Name of the Institution awarding the above Degree: University of Utah, Salt Lake City, Utah**
    c. **Date degree was granted: 1972**

2. **Fields of specialization: Semiconductor Devices , Process Technology ,& wafer Manufacturing in Mega foundries, Microwave/Wireless, IC design layout and Design services**

3. **Teaching, research and, administrative experience: Over 8 years of teaching at Silicon Valley Technical Institute. Life time Teaching Certificate from State of California, issued in 1972. Over 30 years in Electronics High Tech Industries (Silicon Valley, CA)**

4. **Teaching assignments:**

Professional Scrum Master Level II
Scrum Product Owner Essentials
Project Management Essentials

Faculty Name: Dr. John Michael Williams

1. **Educational Background:**
   a. **Earned Degree: Ph.D. Philosophy**
   b. **Name of the Institution awarding the above Degree: Carbondale, Illinois, 62901**
   c. **Date degree was granted: June 1980**
2. **Fields of specialization: Information Technology, Verilog, C, C++, Digital Design**

3. **Teaching, research and, administrative experience: Over 5 years teaching experience in Silicon Valley Technical Institute. Over 25 years of experience in high-tech industry in area of high-Level design methodologies.**

4. **Teaching assignments:**

VLSI Physical Design Essentials

Faculty Name: Dr. Ali Iranmanesh

1. **Educational Background:**
   a. **Earned Degree: Ph.D., Electronics and Physics**
   b. **Name of the Institution awarding the above Degree: Stanford University**
   c. **Date degree was granted: June 1984**
2. **Fields of specialization: Semiconductor Technology, Device Physics, IC Circuits Design**

3. **Teaching, research and, administrative experience: Over 10 years teaching experience in Silicon Valley Technical Institute. Over 25 years of experience in high-tech industry in area of IC circuit design and semiconductor technology.**

4. **Teaching assignments for the current year:**

Lean Manufacturing Essentials
Custom Physical Design Essentials
Analog IC Design

Faculty Name: Fred Fowler

1. **Educational Background:**
    a. **Earned Degree: BA, History/Econ.**
    b. **Name of the Institution awarding the above Degree: Haverford College**
    c. **Date degree was granted: 1979**
2. **Fields of specialization: Computer Science, Management Theory, Agile Software Development, The Scrum Framework.**

3. **Teaching, research and, administrative experience: Mr. Fowler has been teaching the Scrum Framework since March, 2015 and has the highest certification level available (PSM III from Scrum.org). He is one of just over 300 people worldwide to have earned this certification. He is also a former Vice President and CIO, and has provided corporate training in the Scrum Framework for more than 300 students in California, India, China, Vietnam and Central America.**

4. **Teaching assignments for the current year:**

    Scrum Master and Jira Training
    Professional Scrum Master Level II
    Professional Scrum Developer Training

Faculty Name: NEELAM DABHOLKAR

1. **Educational Background:**
    a. **Earned Degree: Bachelor of Engineering**
    b. **Name of the Institution awarding the above Degree: Mumbai University**
    c. **Date degree was granted: June 1998**
2. **Fields of specialization: Product Management, Scrum, PMP**

3. **Teaching, research and, administrative experience: Total experience of 17 years that includes software development and 5 years of teaching.**

4. **Teaching assignments for the current year:**

    a. **Scrum Master and Jira Training**
    b. **Professional Scrum Master Level II**
    c. **Professional Scrum Developer Training**

Faculty Name: Marilenis Lee

1. **Educational Background:**
    a. **Earned Degree: BSc. Computer Science, MSc. Computer Science, MA. in Multimedia**
    b. **Name of the Institution awarding the above Degree: BSc. and MSc.: Universidad Simon Bolivar - Venezuela. MA.: California State University East Bay**
    c. **Date degree was granted: BSc.: January 1992, MSc.: September 1998, MA.: July 2001**

2. **Fields of specialization: Computer Graphics, Multimedia and Web Development**

3. **Teaching, research and, administrative experience: More than 10yrs of teaching experience. 25 years of professional experience**

4. **Teaching assignments for the current year:**

    a. **Python Programming Essentials**
    b. **JavaScript Programming Essentials**

Faculty Name: Amy Federowicz

5. **Educational Background:**
    a. **Earned Degree: Bachelor of Science Degree**
    b. **Name of the Institution awarding the above Degree: New England Institute of Technology**
    c. **Date degree was granted: BSc.: September 2009**

6. **Fields of specialization: Architectural/Building Engineering Technology**

7. **Teaching, research and, administrative experience: Adjunct Instructor at ITT Technical Institute, December 2015 - September 2016**

8. **Teaching assignments for the current year:**

    c. **Computer Aided Design and Drafting with AutoCAD**
    d. **SketchUp Essentials**